

FIG.4(A)

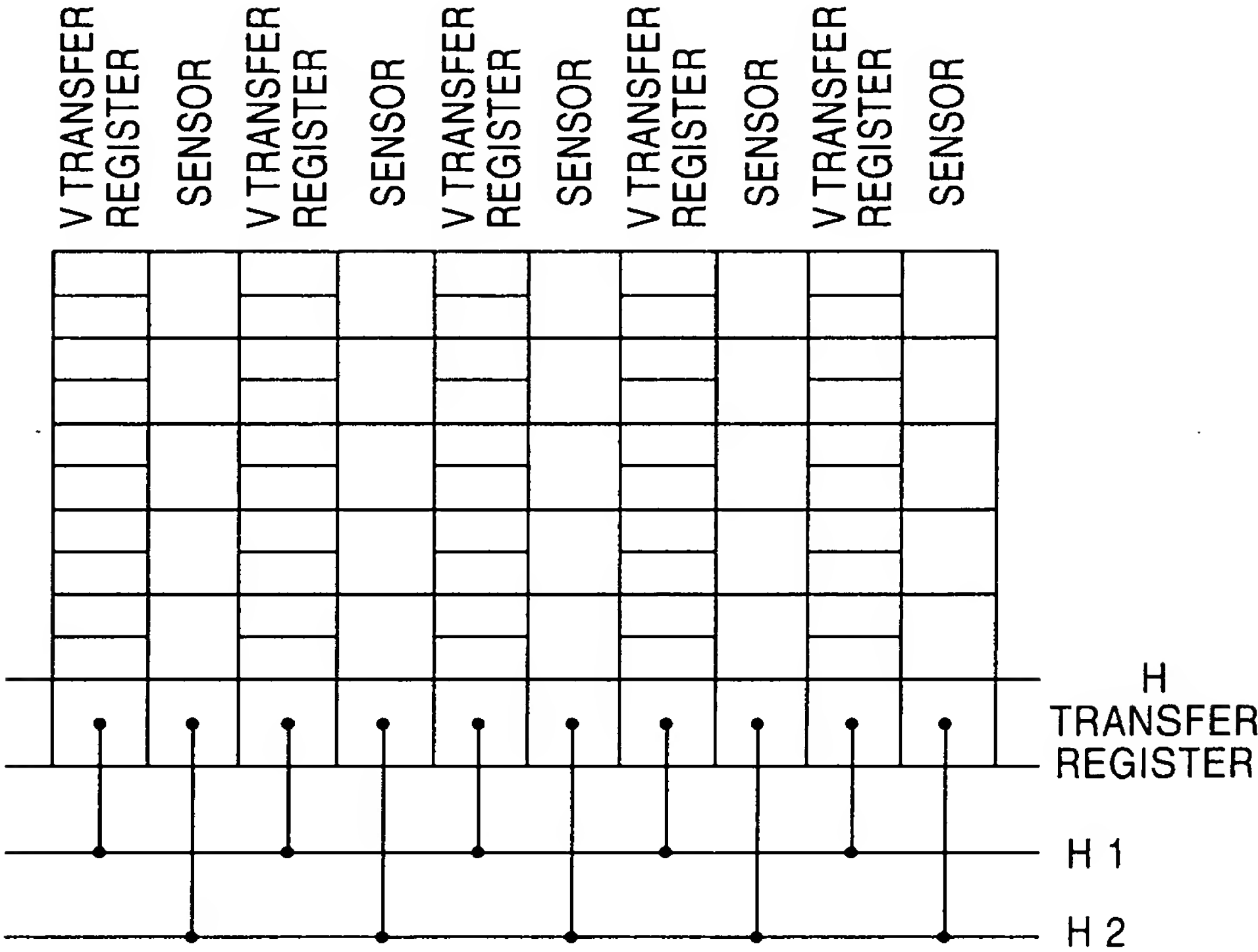


FIG.4(B)

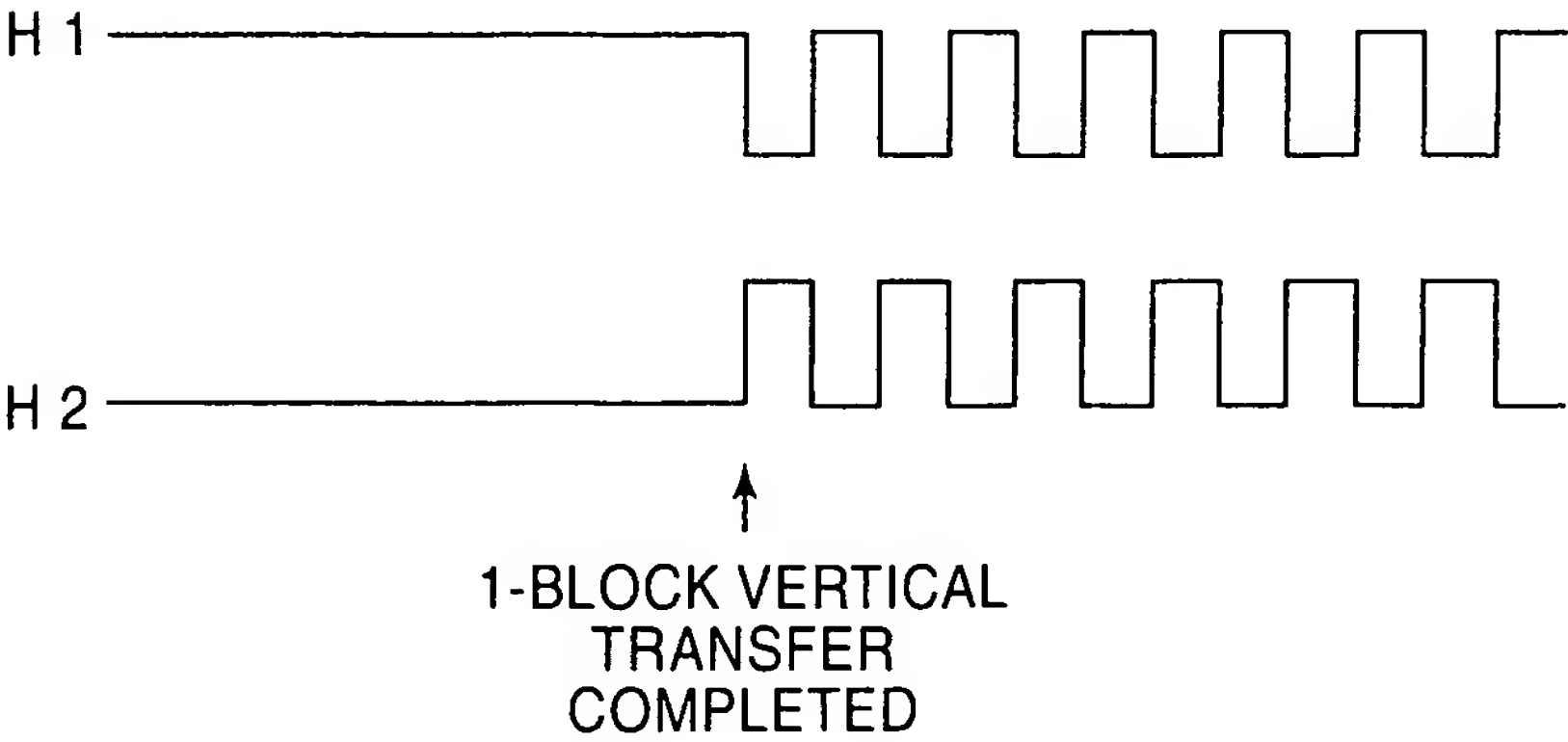


FIG. 5

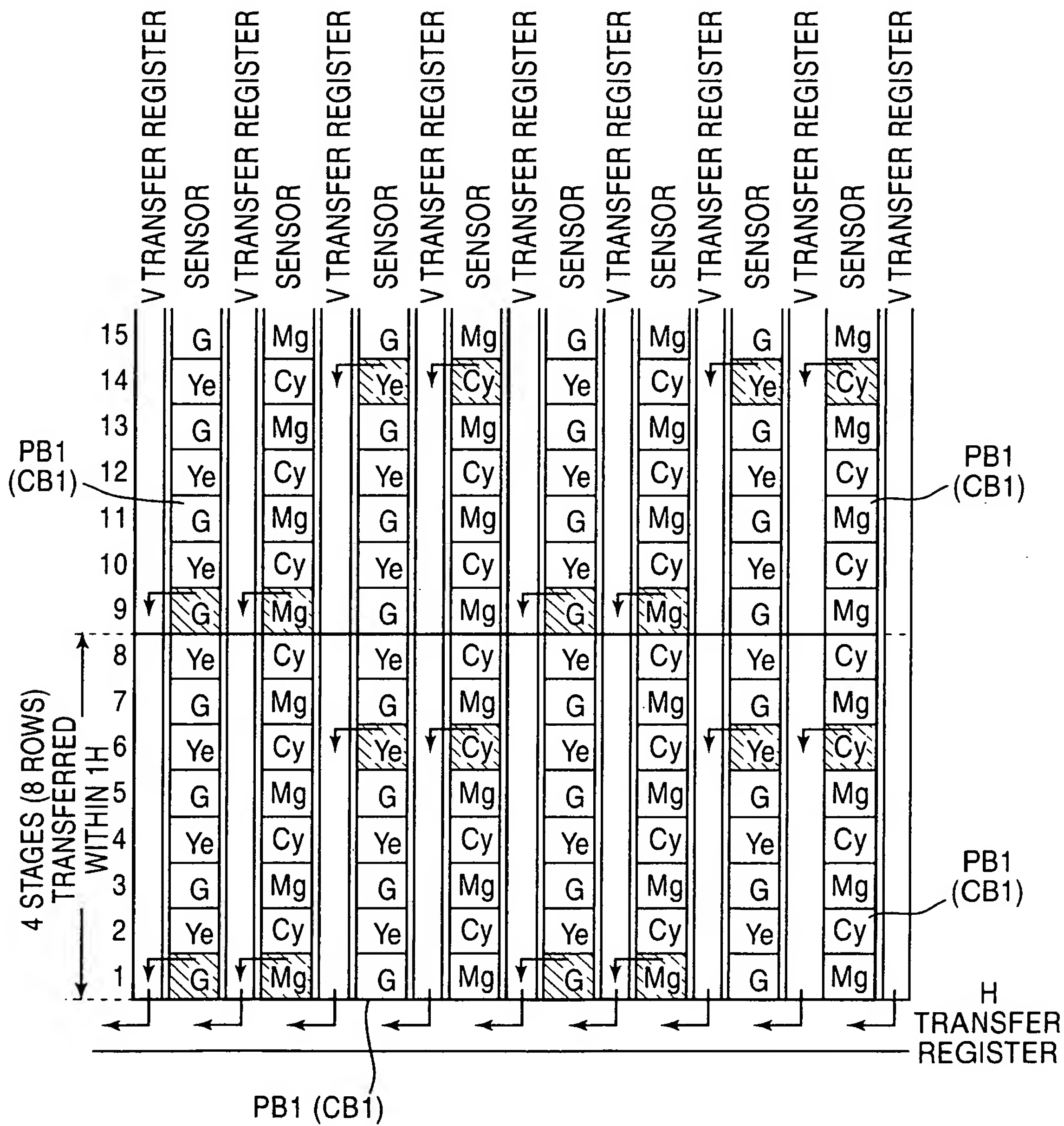


FIG.6(A)

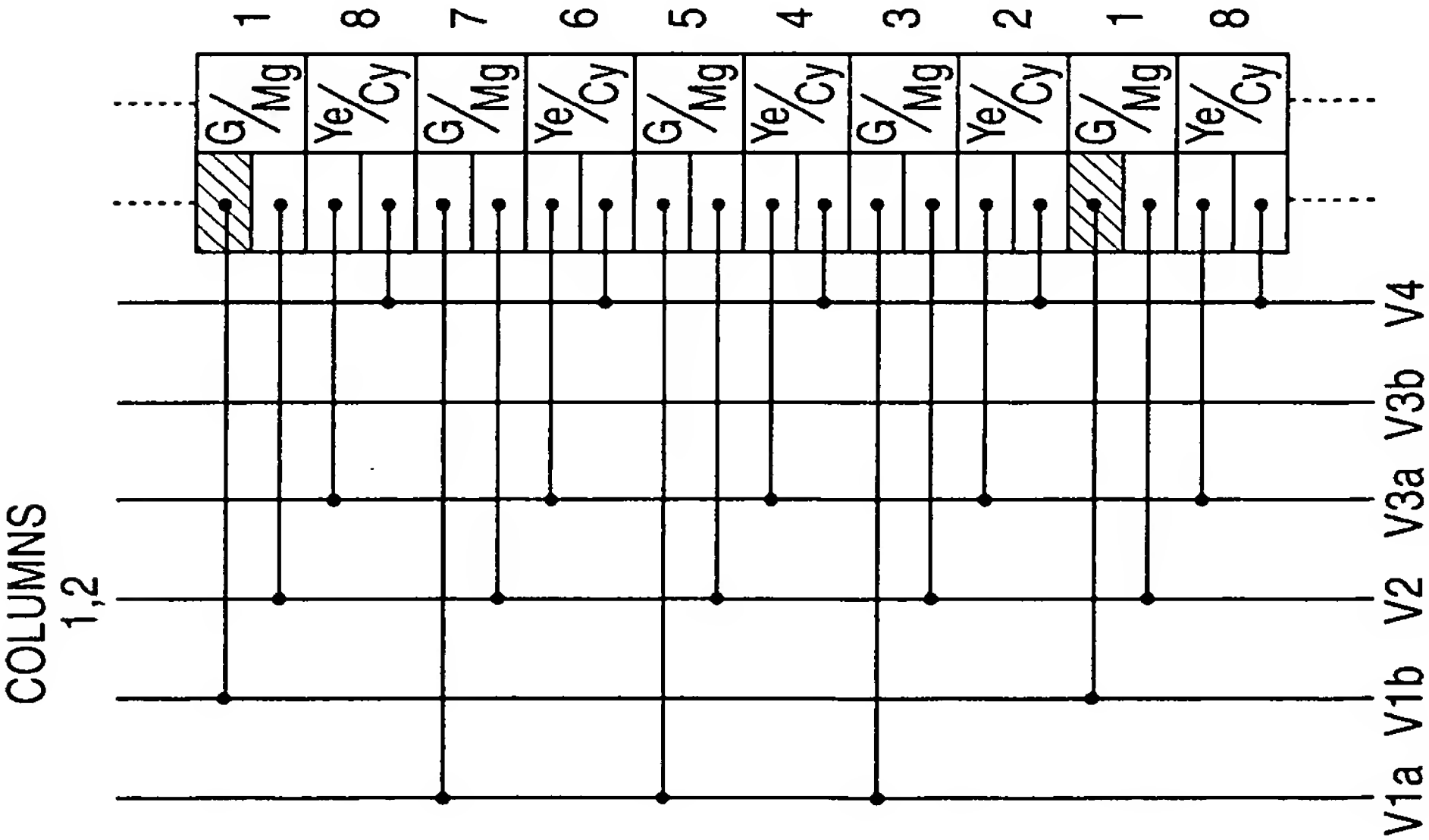


FIG.6(B)

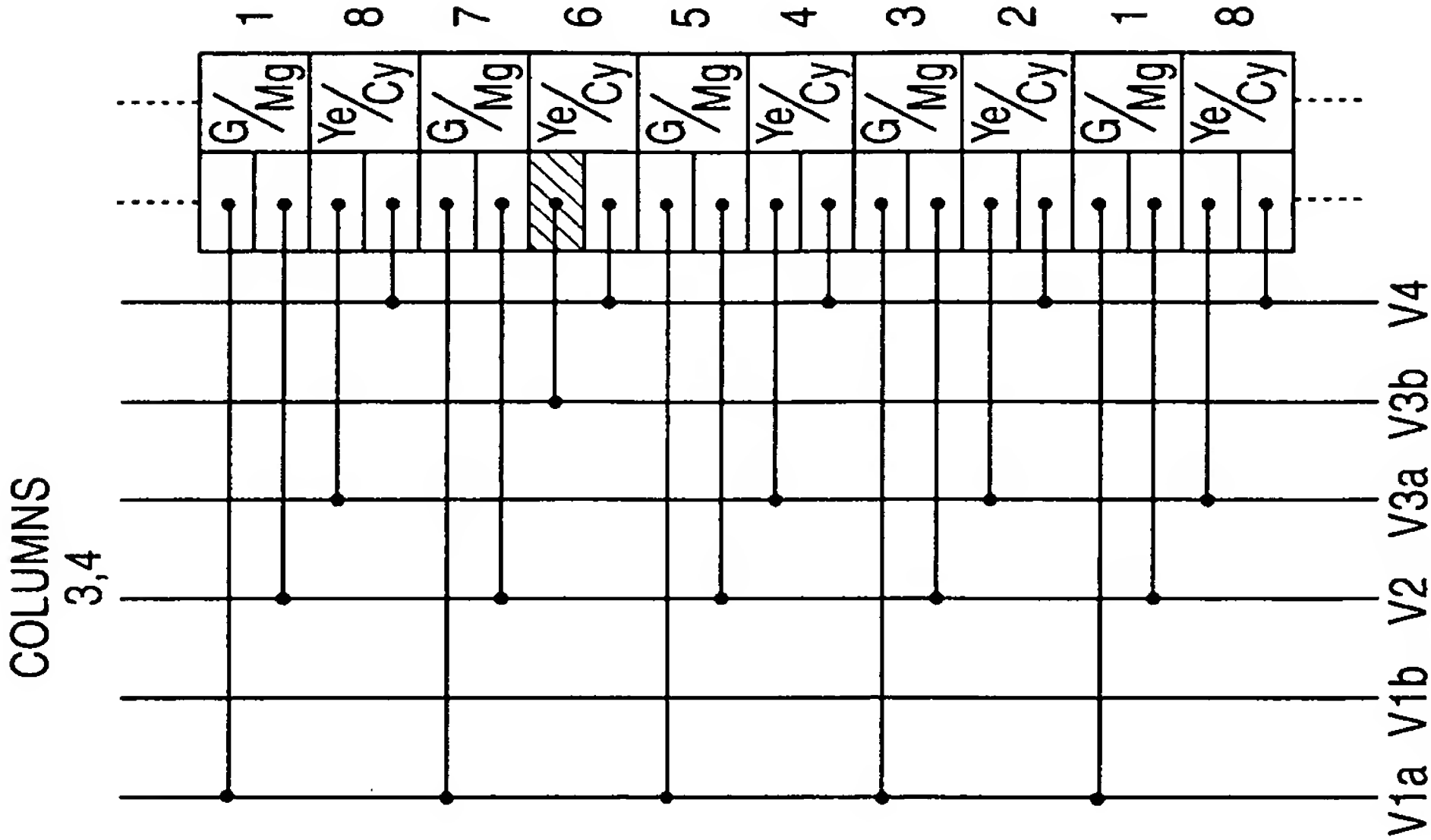
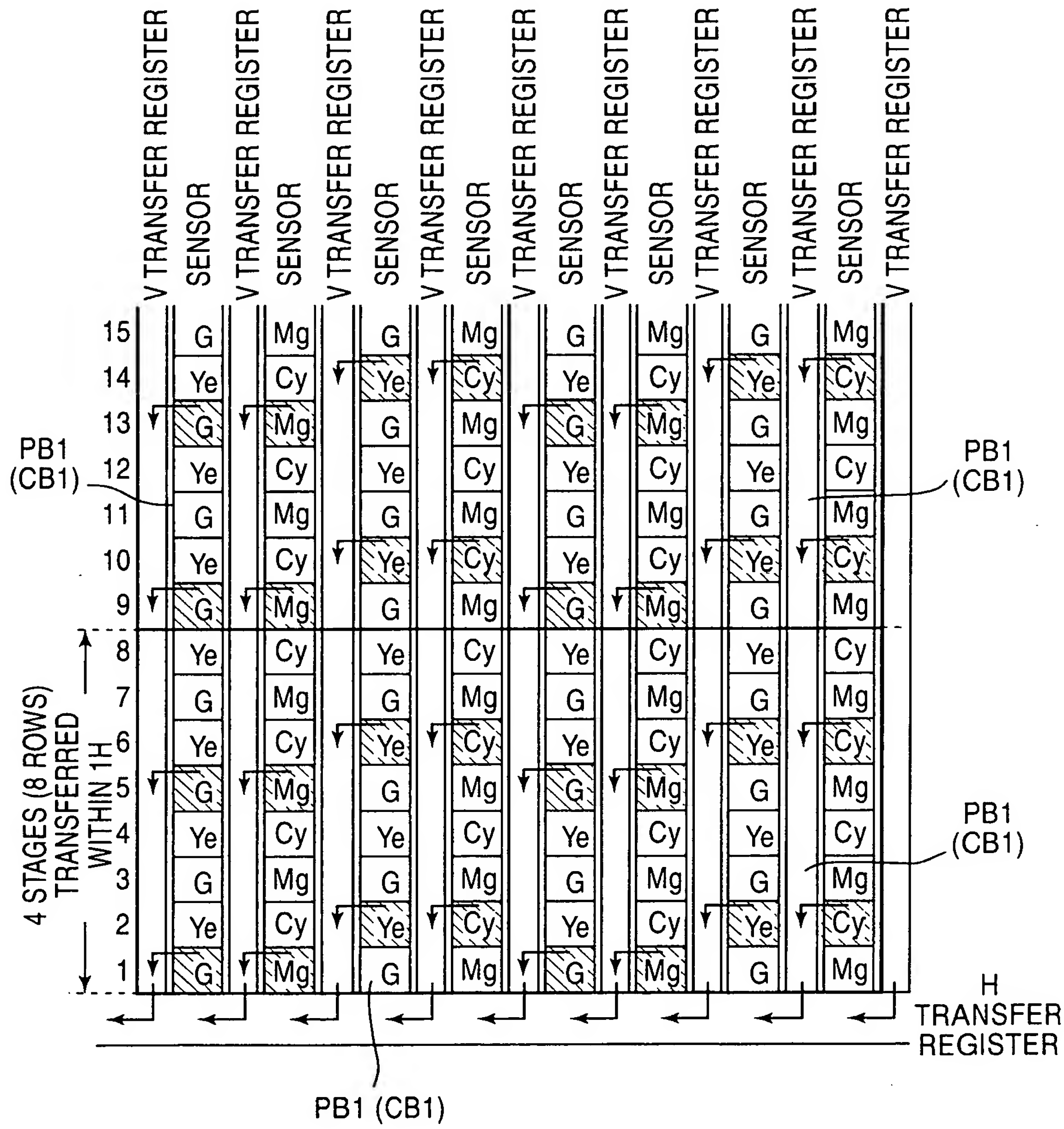




FIG.8



COLUMNS  
1,2



COLUMNS  
3,4

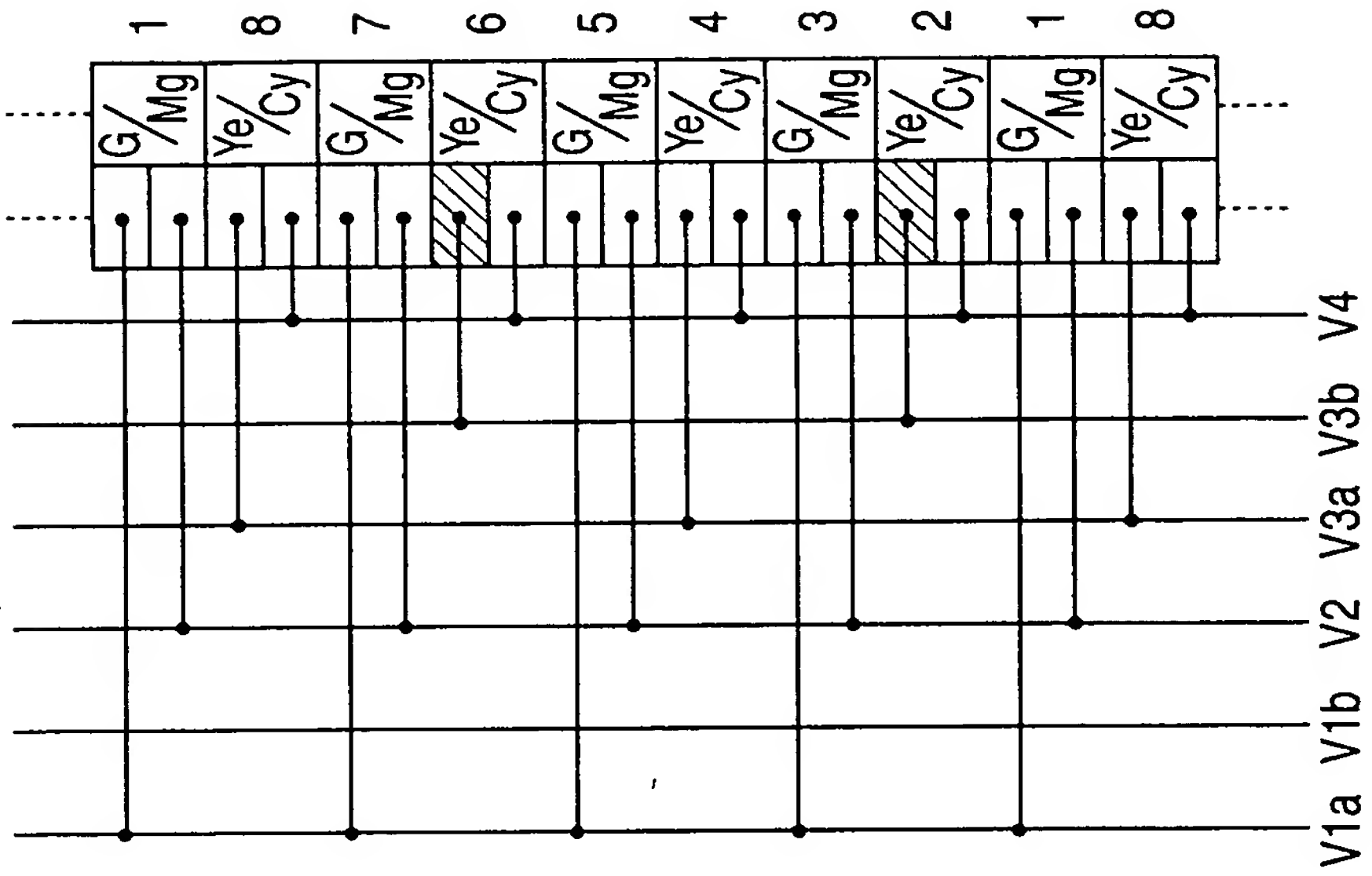








FIG. 11

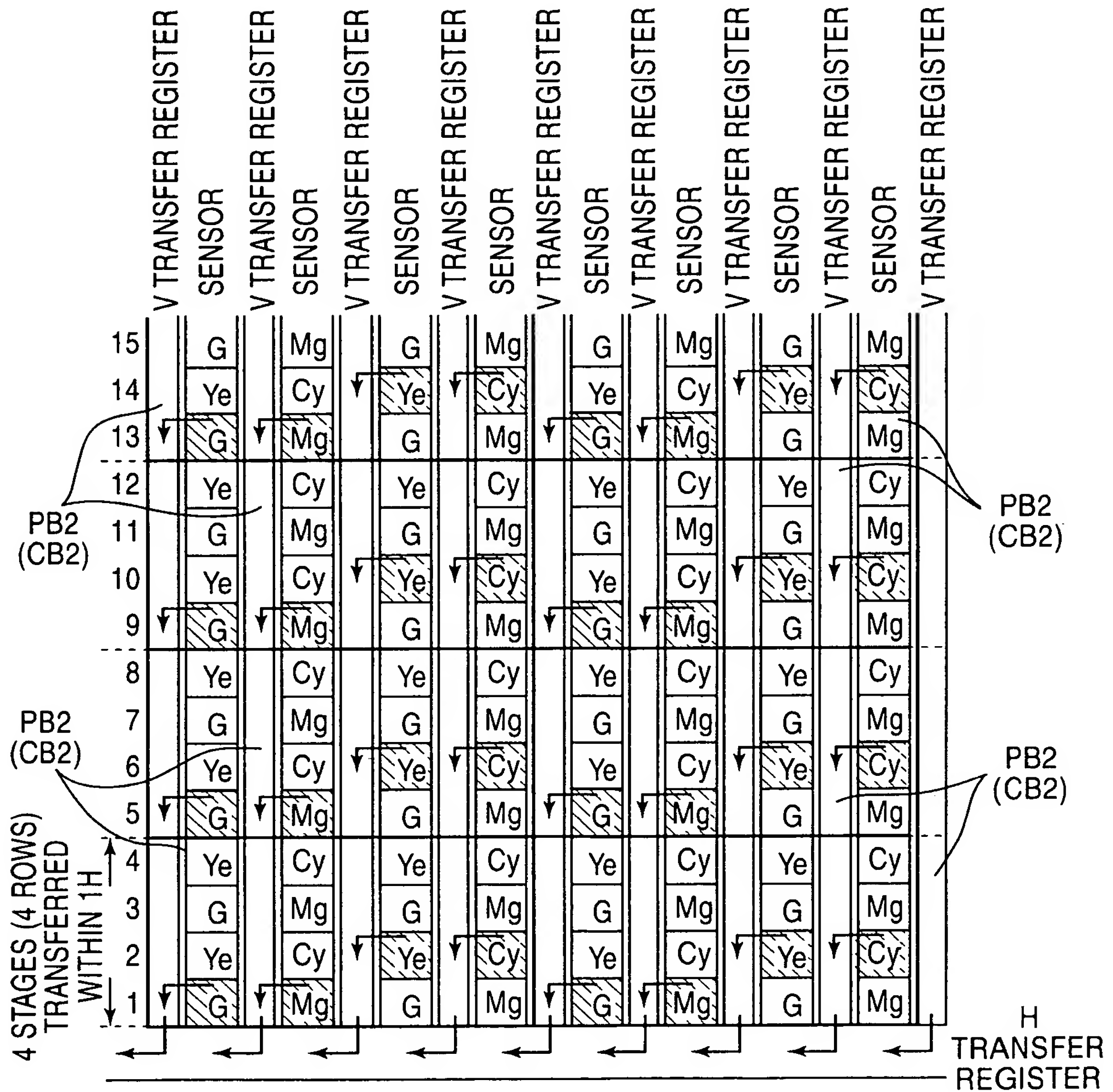


FIG.12(A)

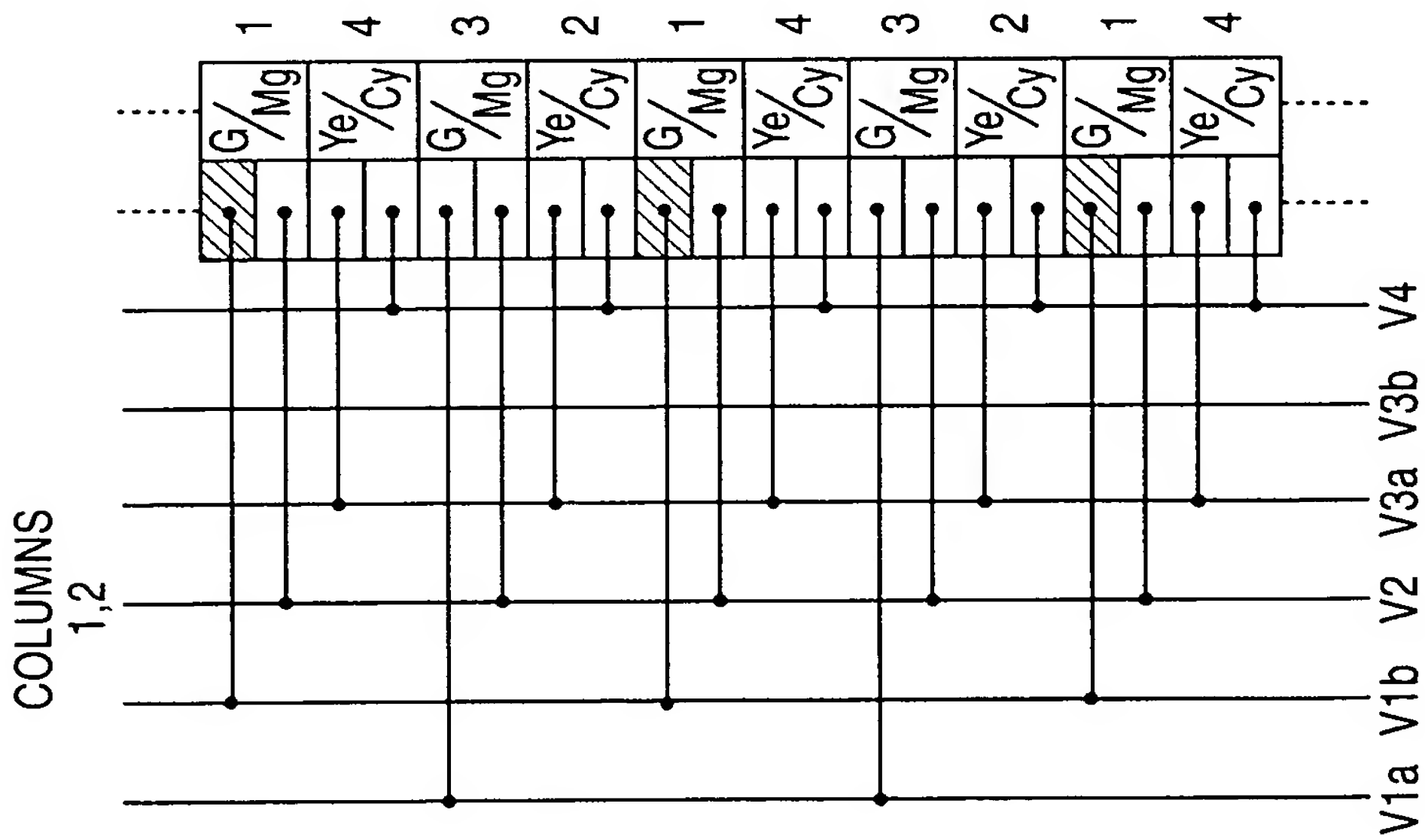


FIG.12(B)

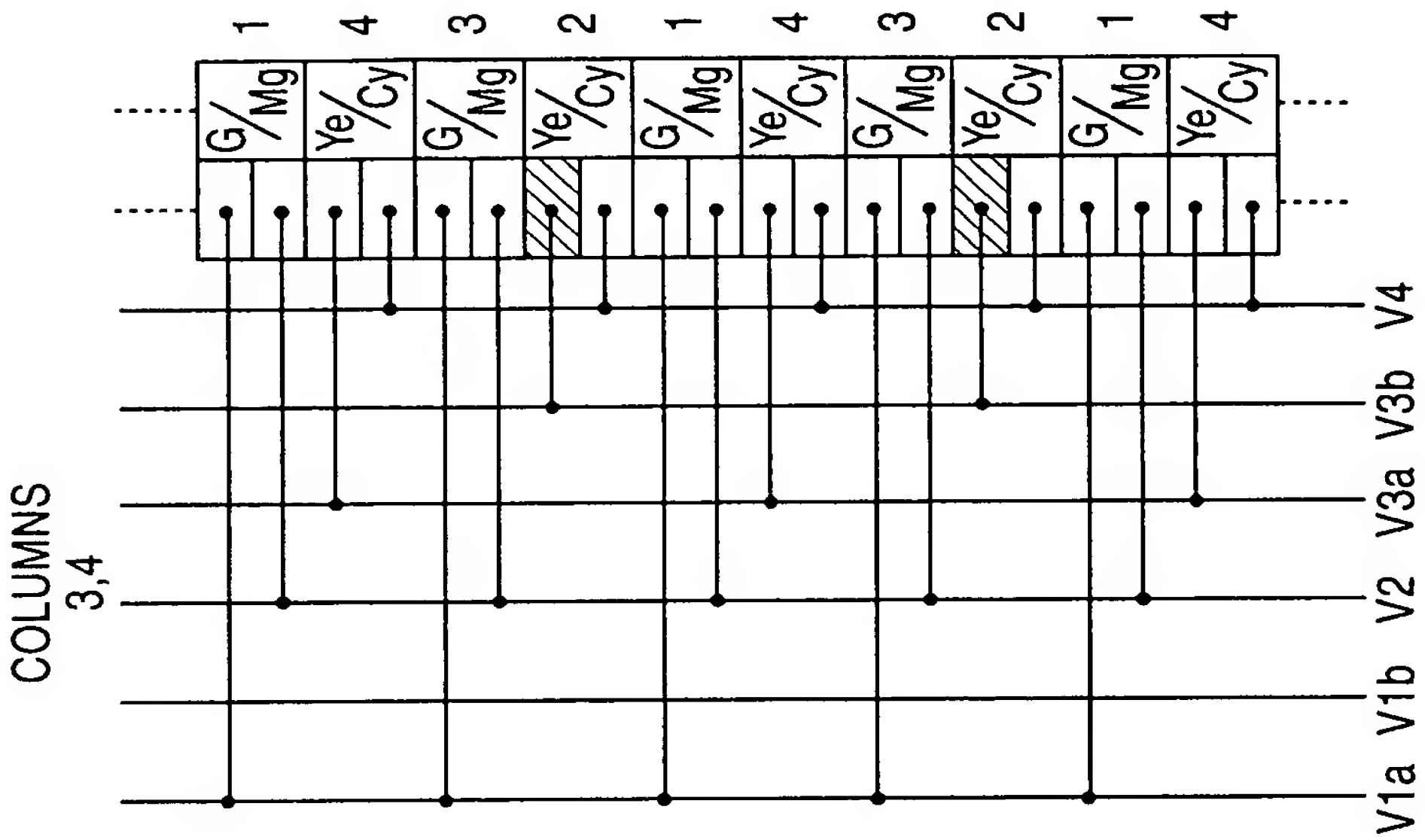


FIG. 13(A)

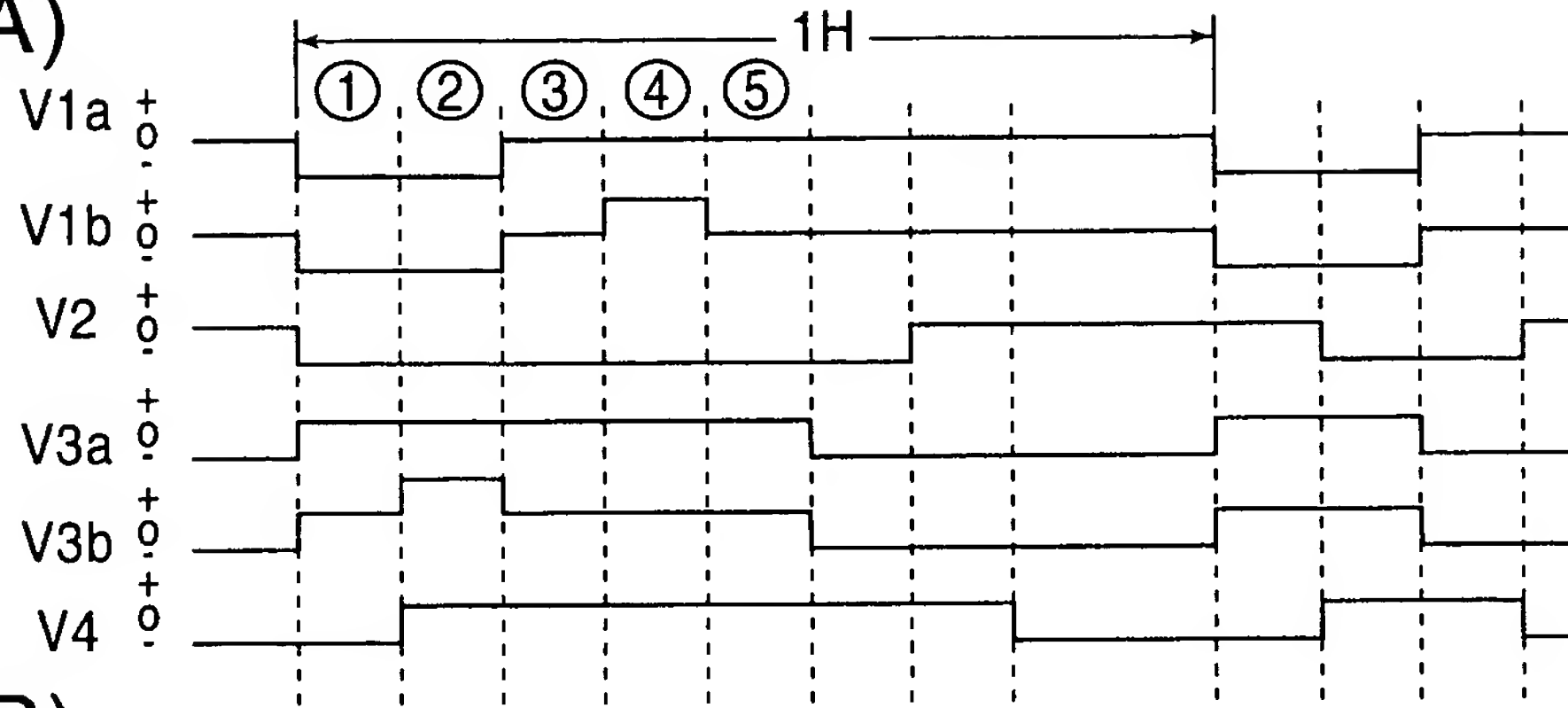


FIG. 13(B)

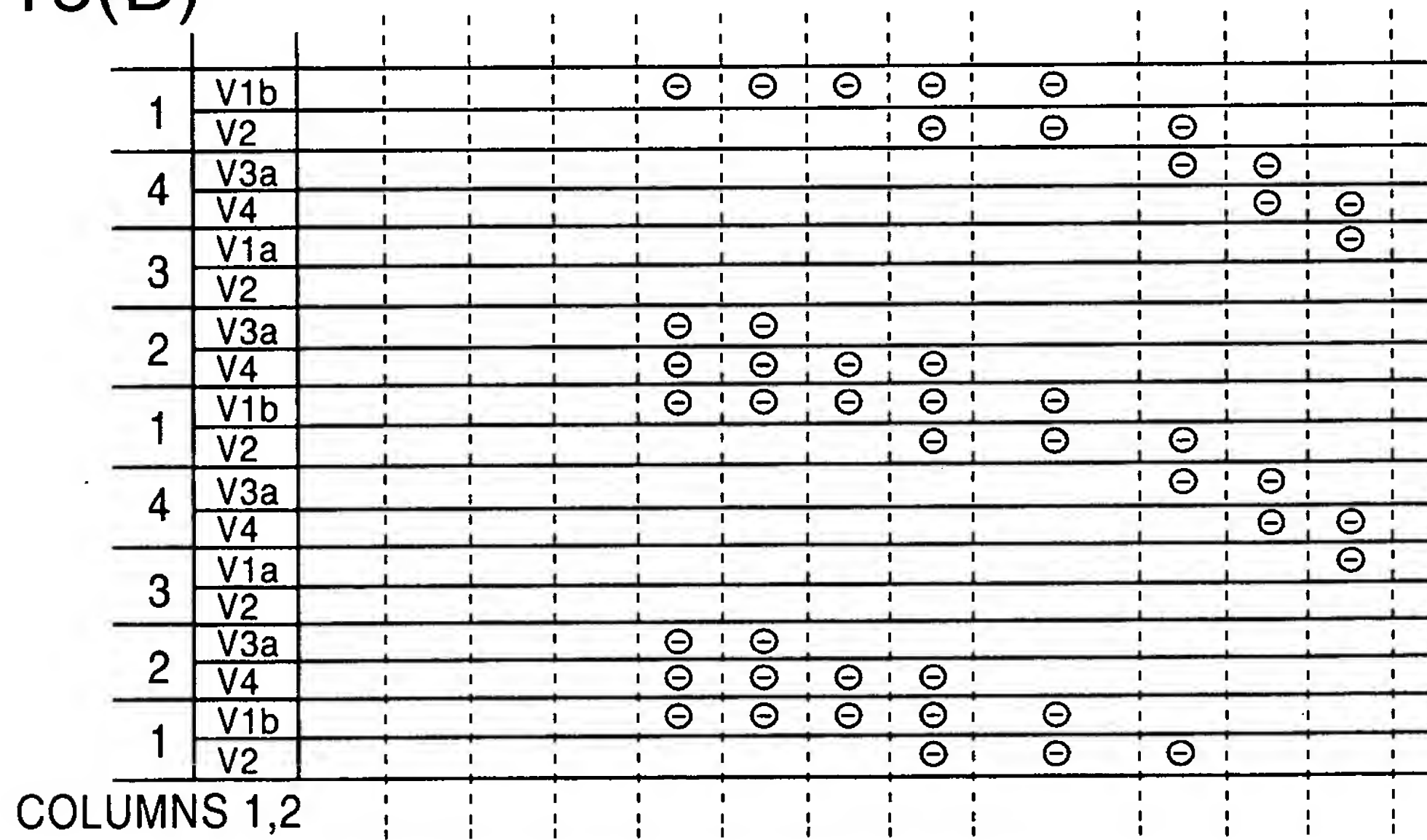


FIG. 13(C)

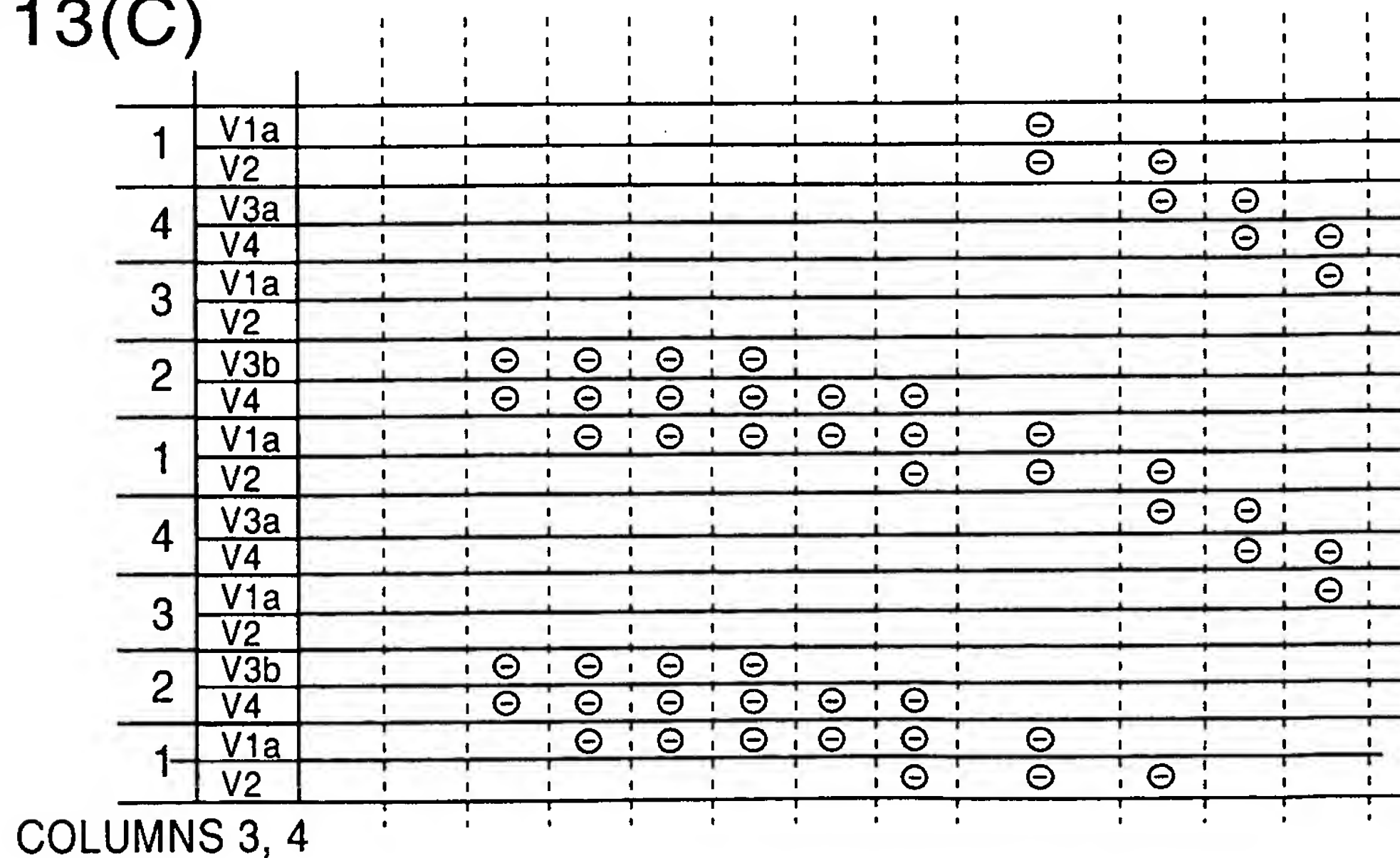


FIG. 14

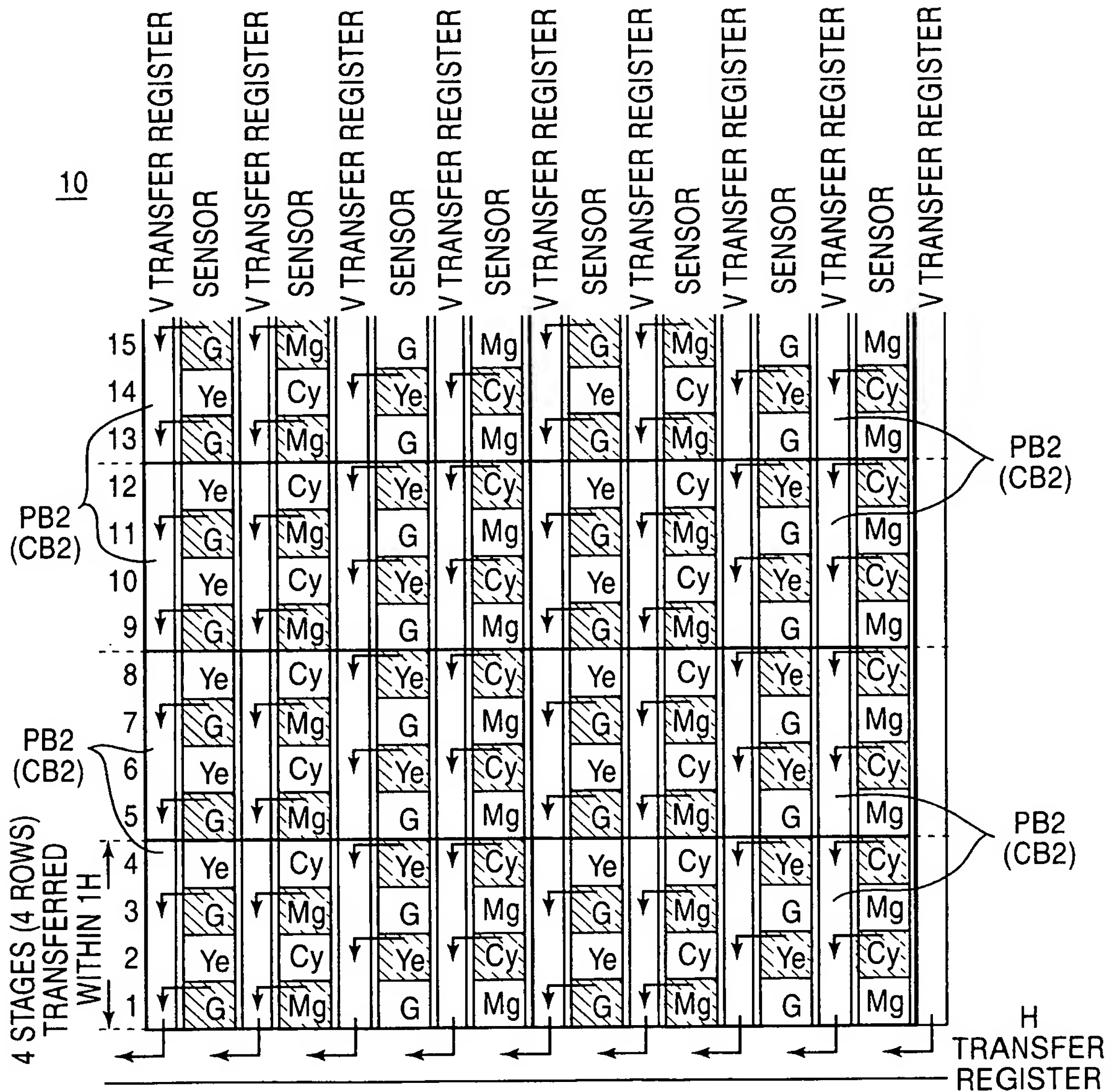


FIG.15(A)

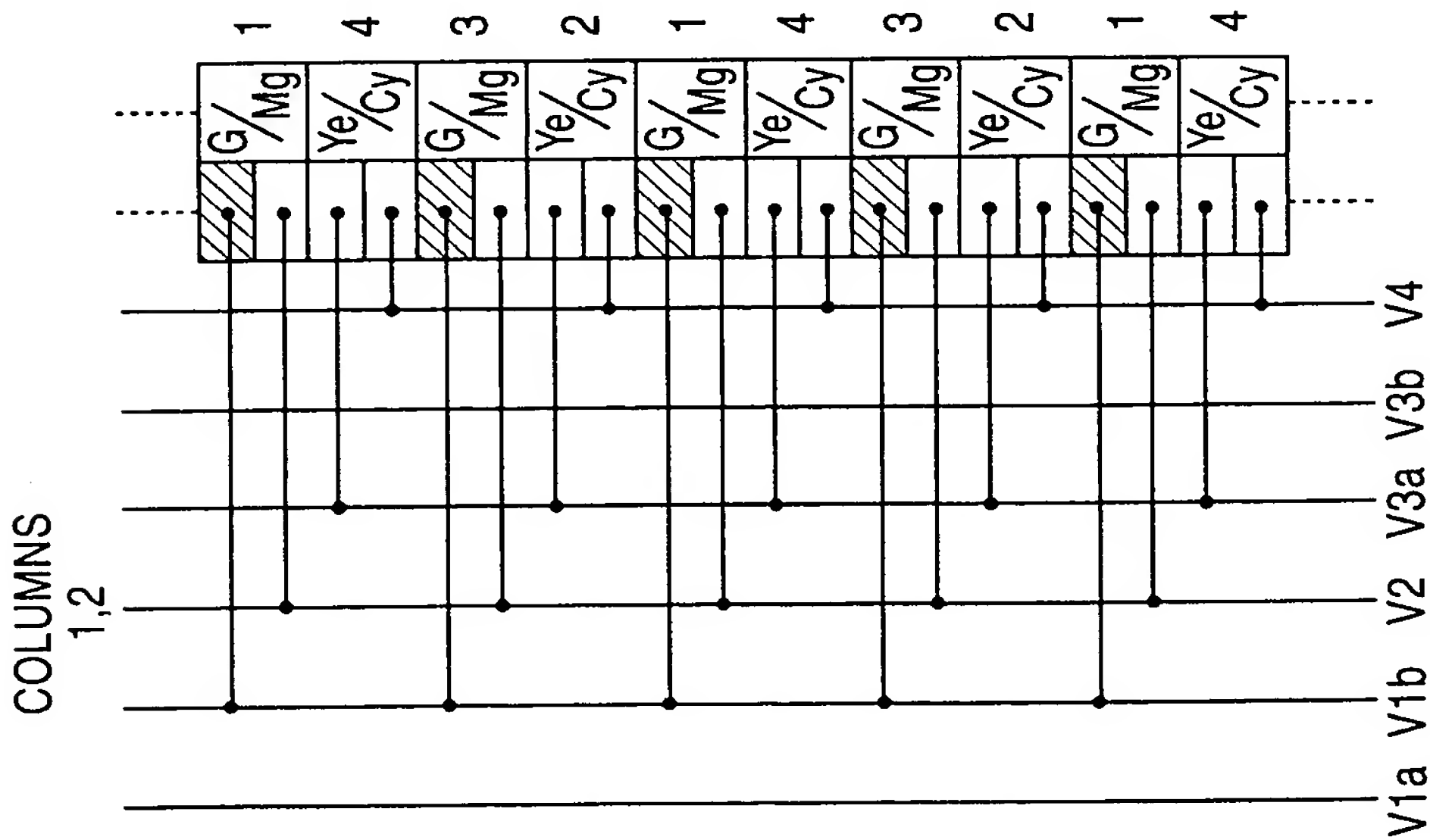


FIG.15(B)

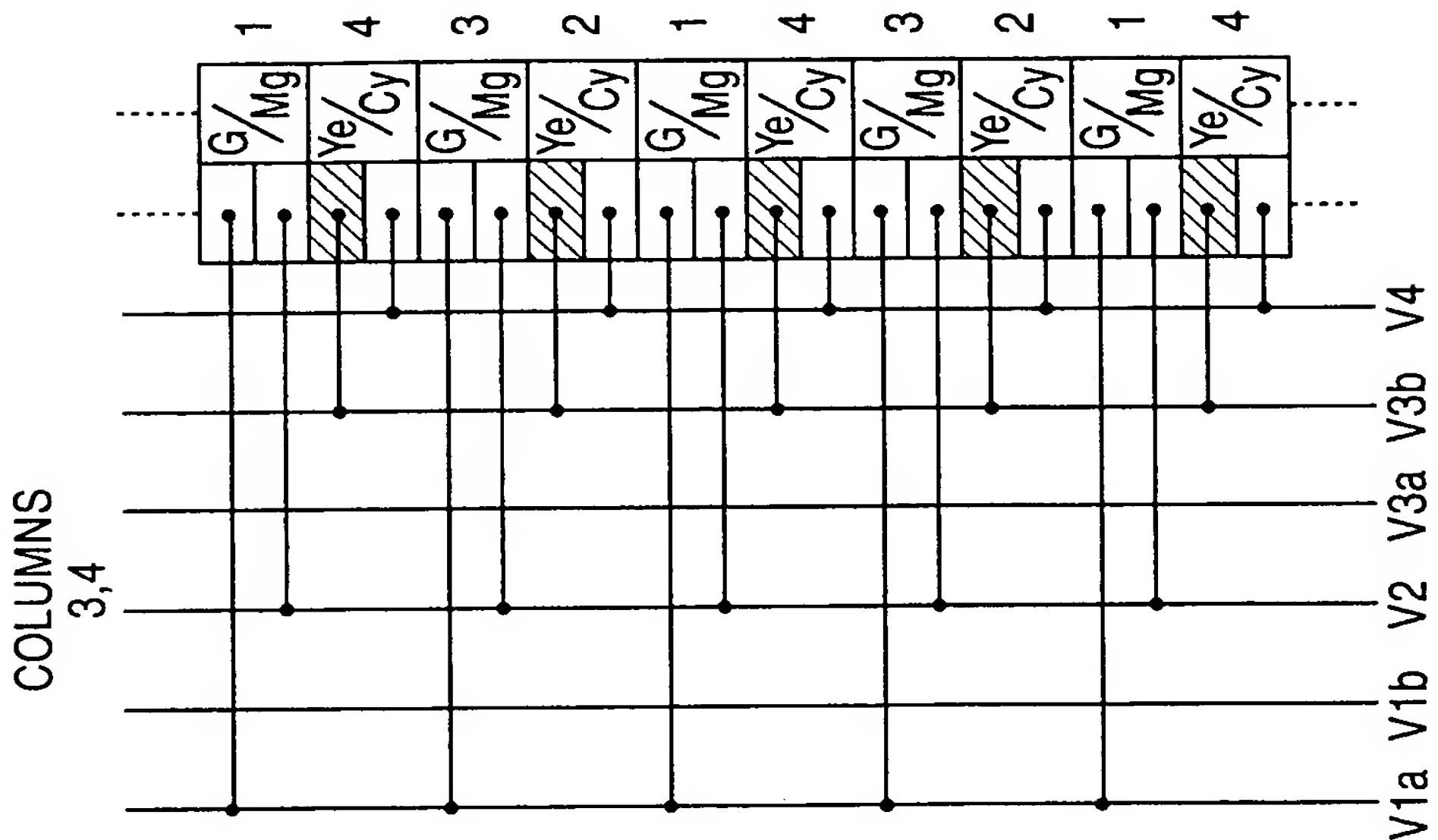


FIG. 16(A)

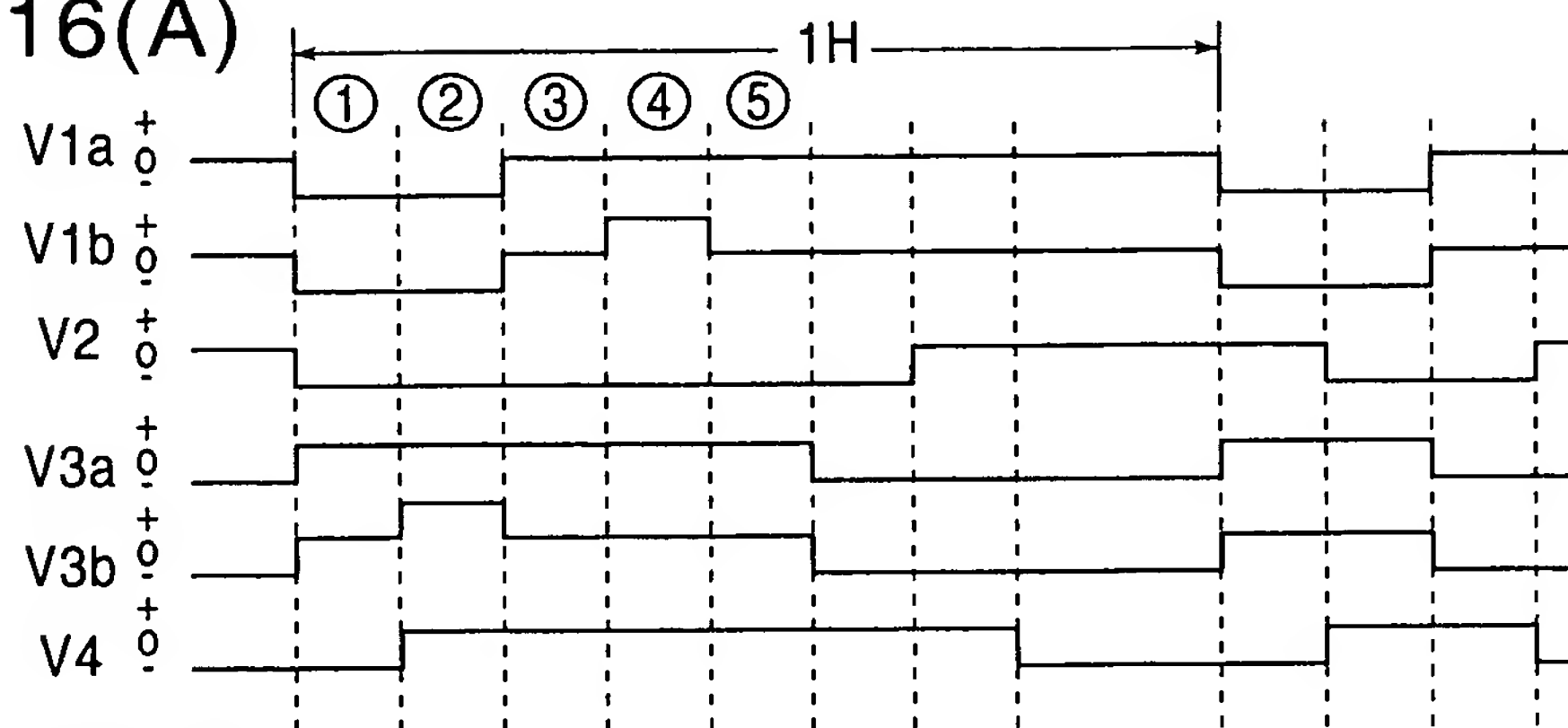


FIG. 16(B)

[illegible]

COLUMNS 1,2

FIG.16(C)

[illegible]

COLUMNS 3, 4



FIG. 17

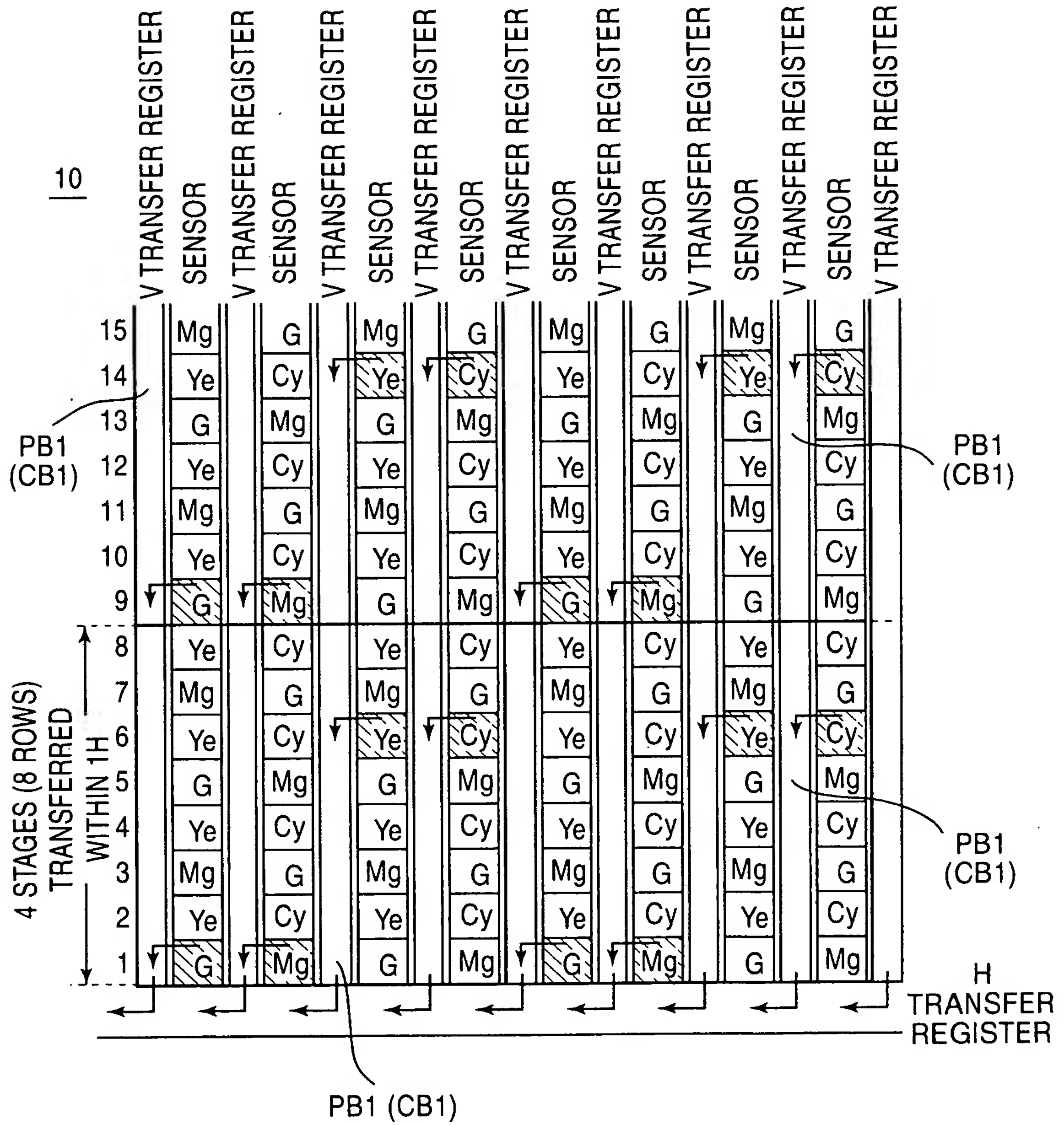




FIG.18(B)

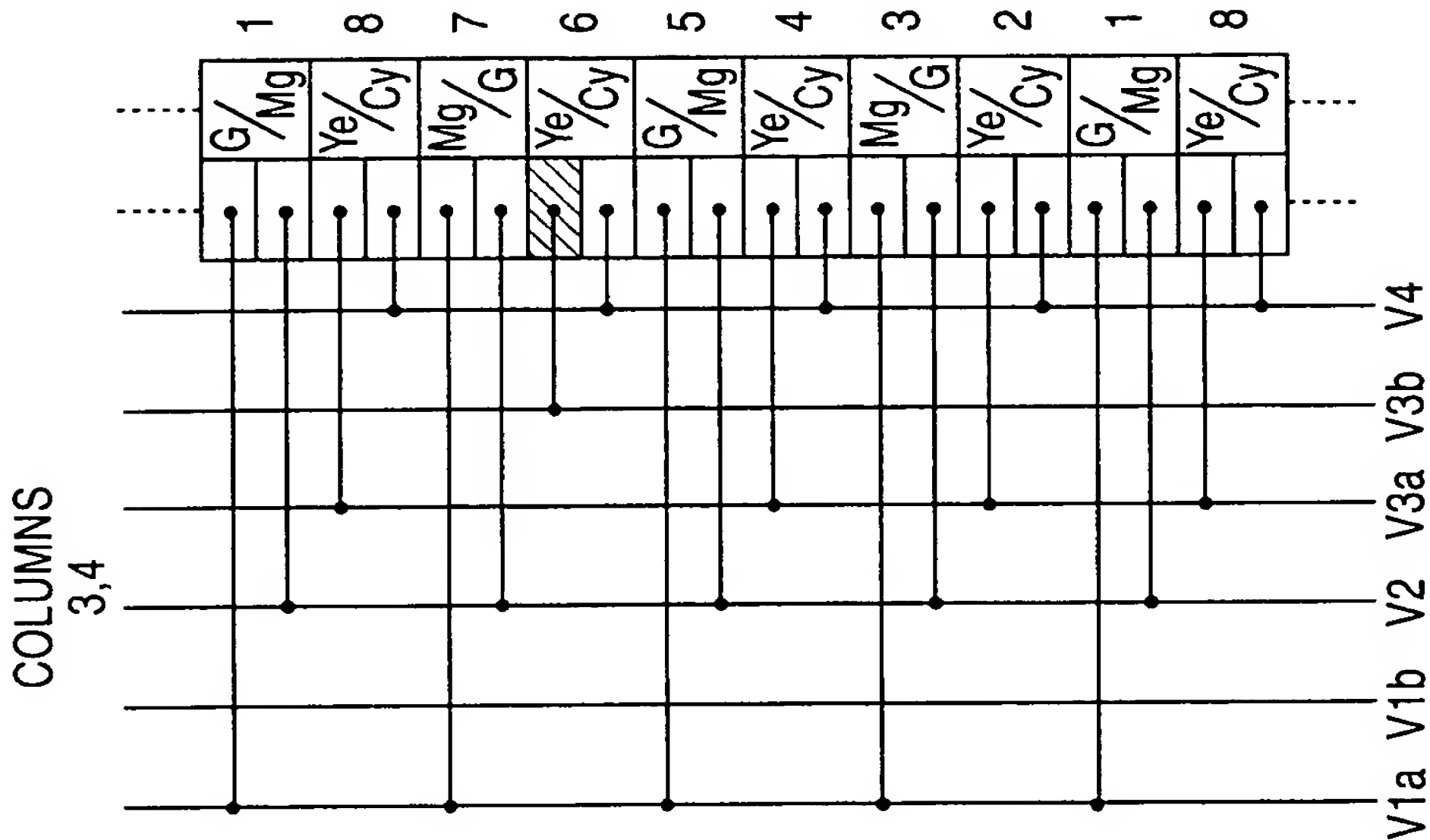


FIG.18(A)

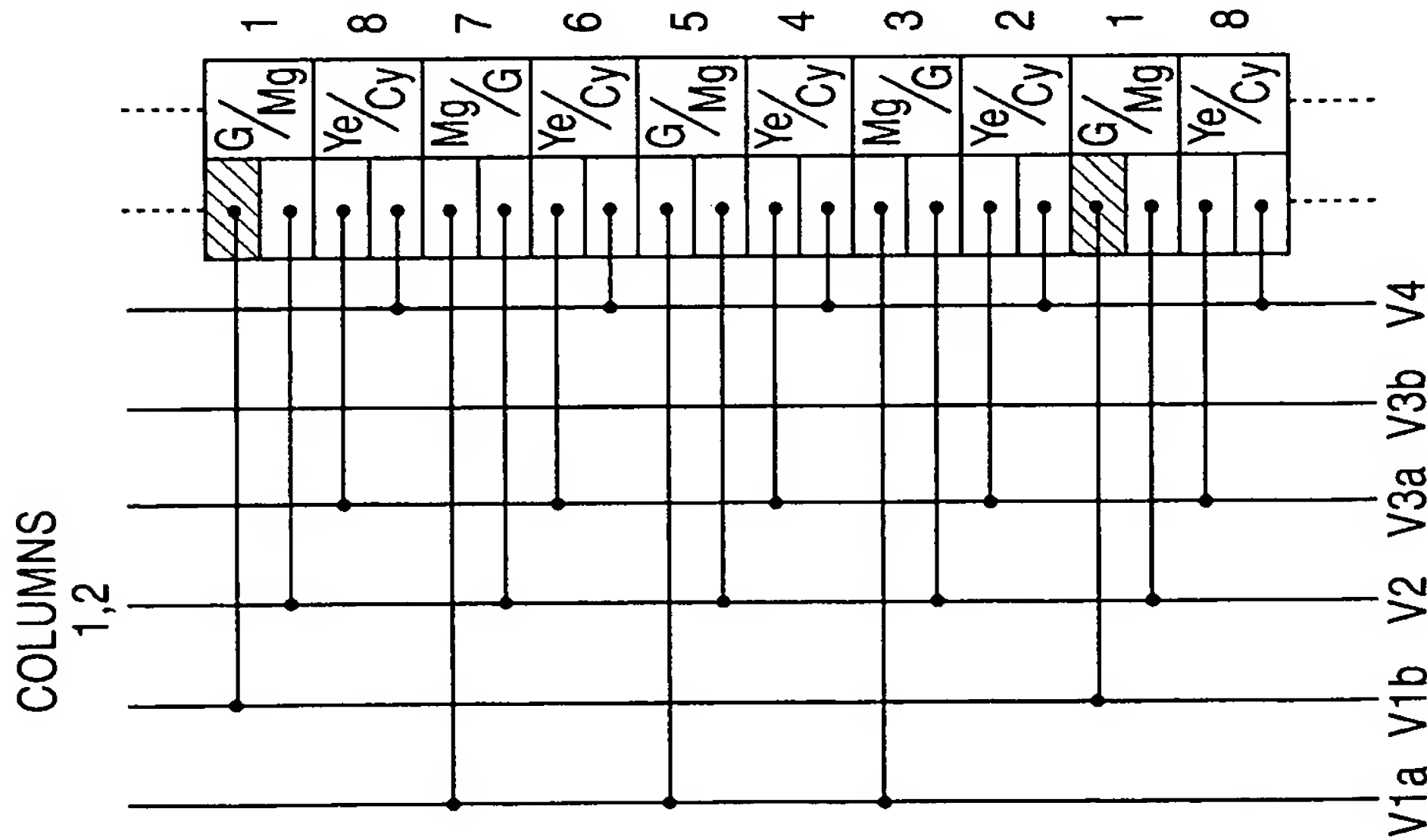




FIG.20

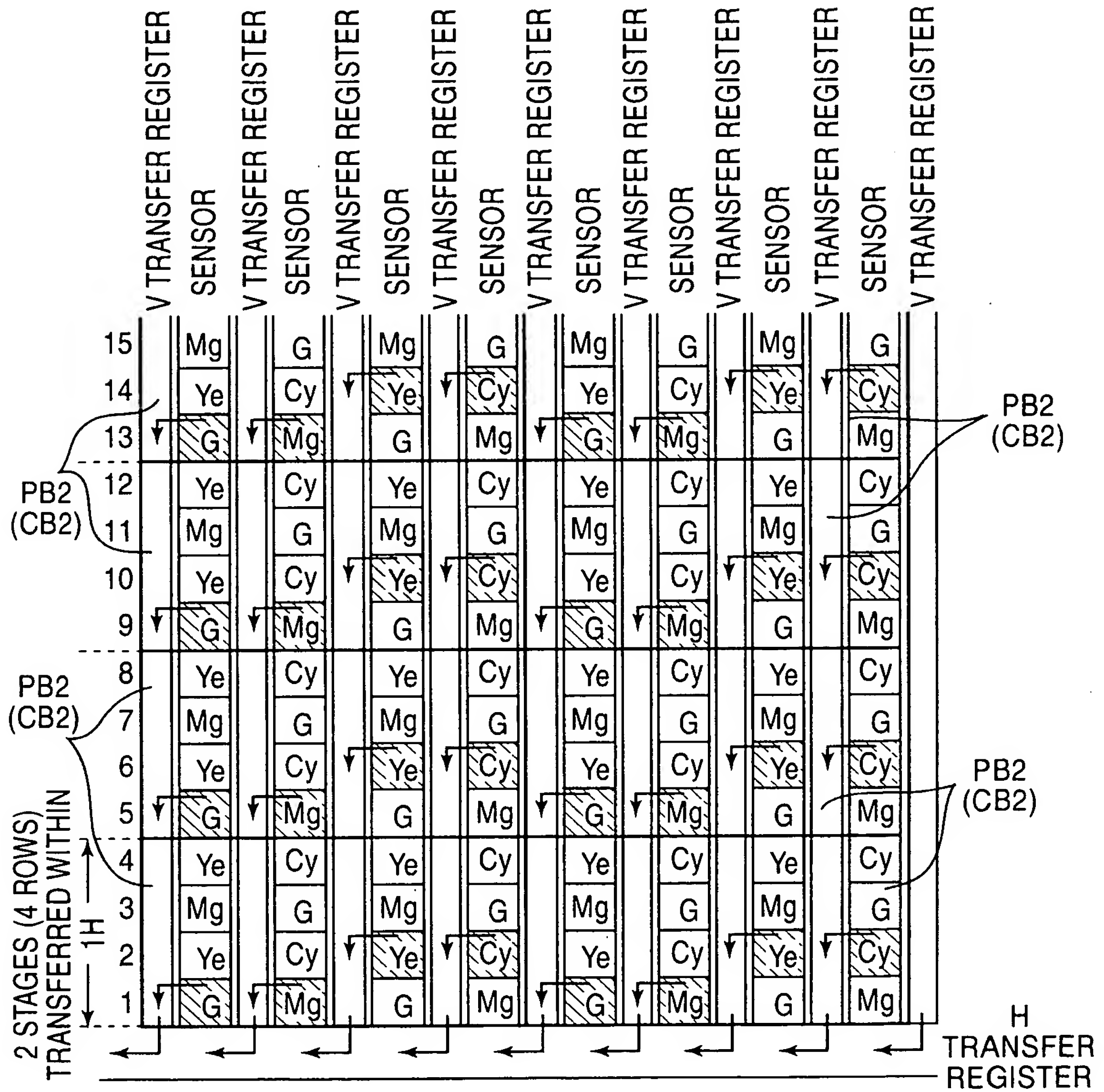


FIG.21(A)

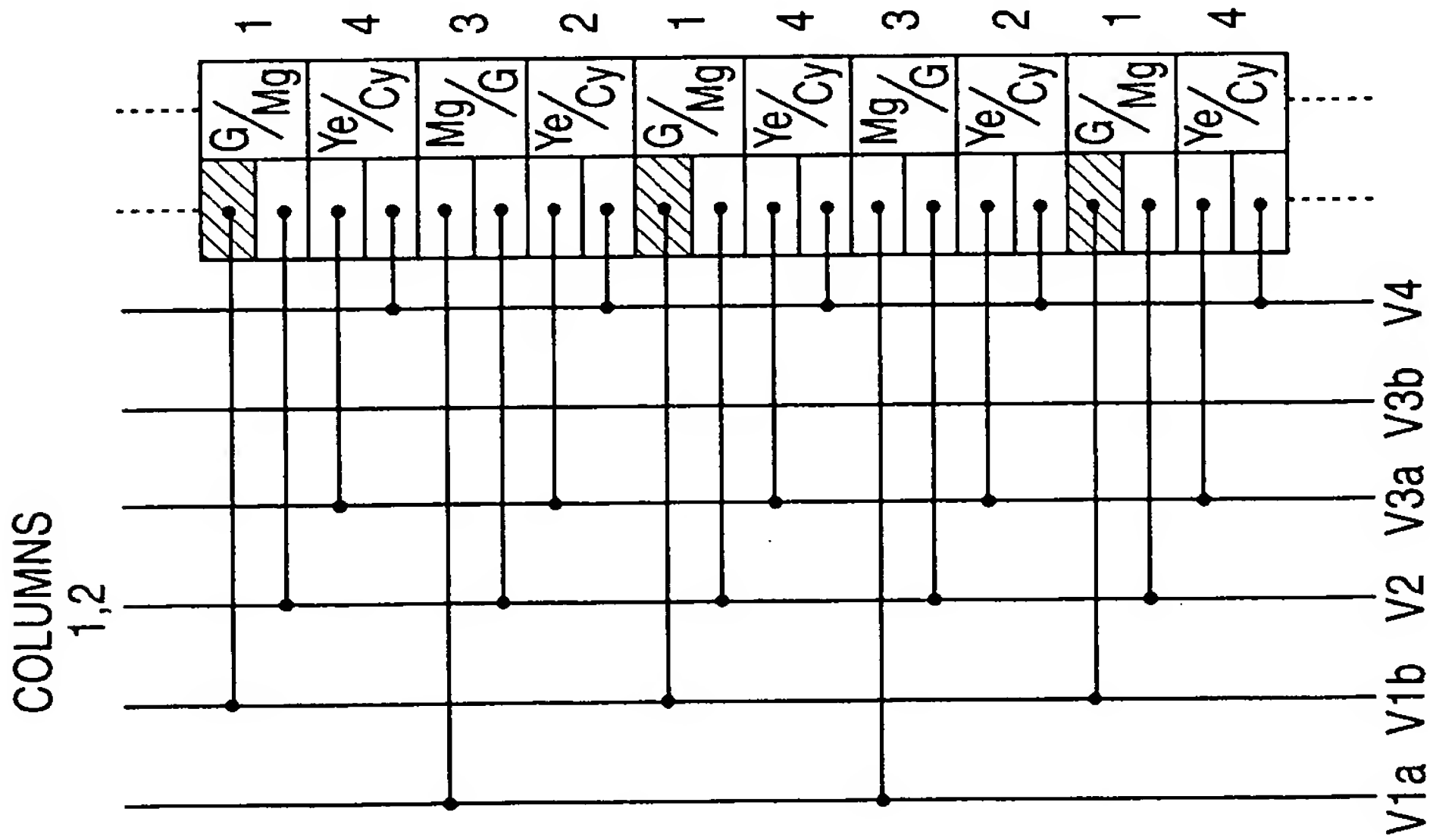


FIG.21(B)

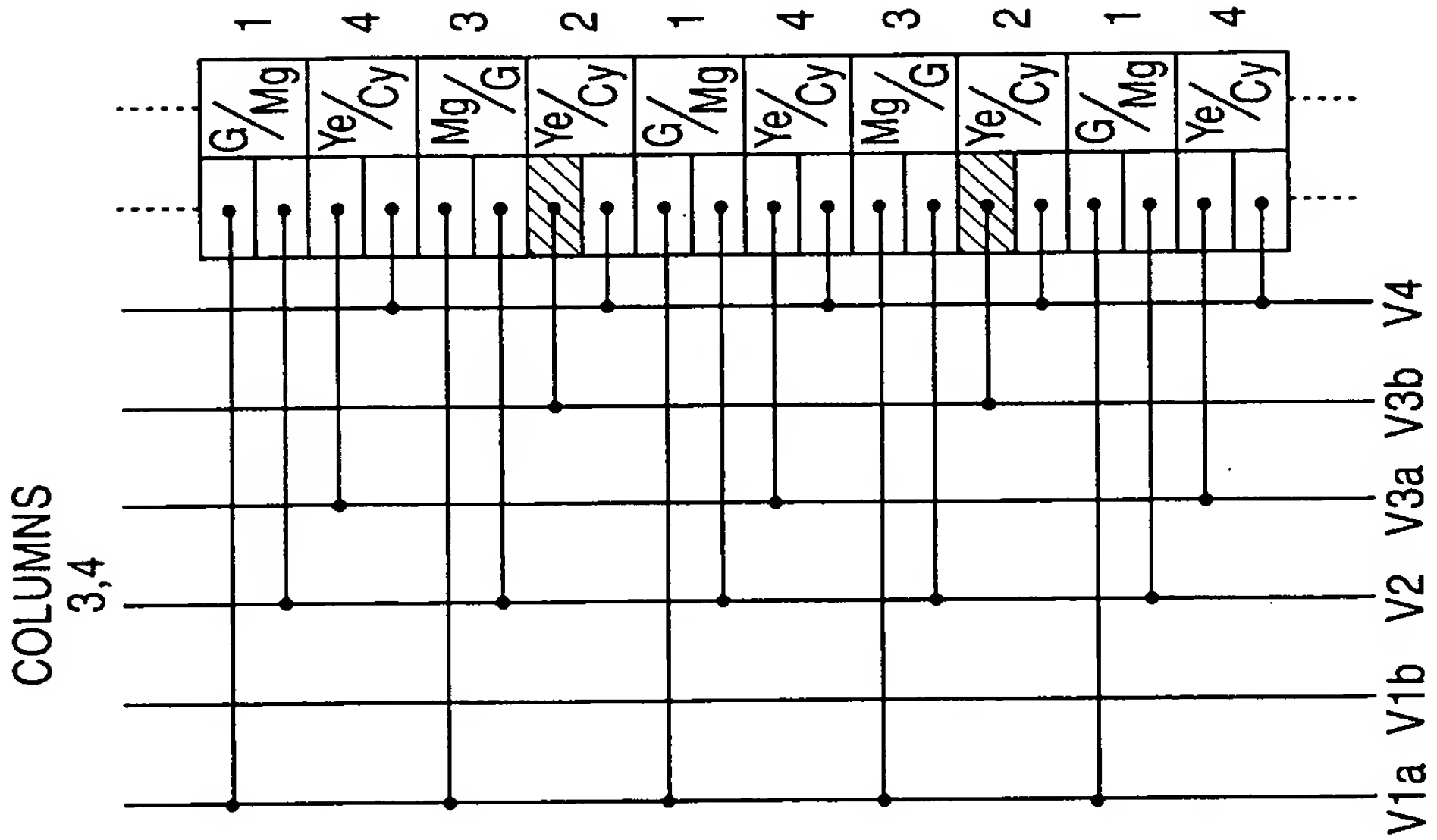


FIG.22(A)

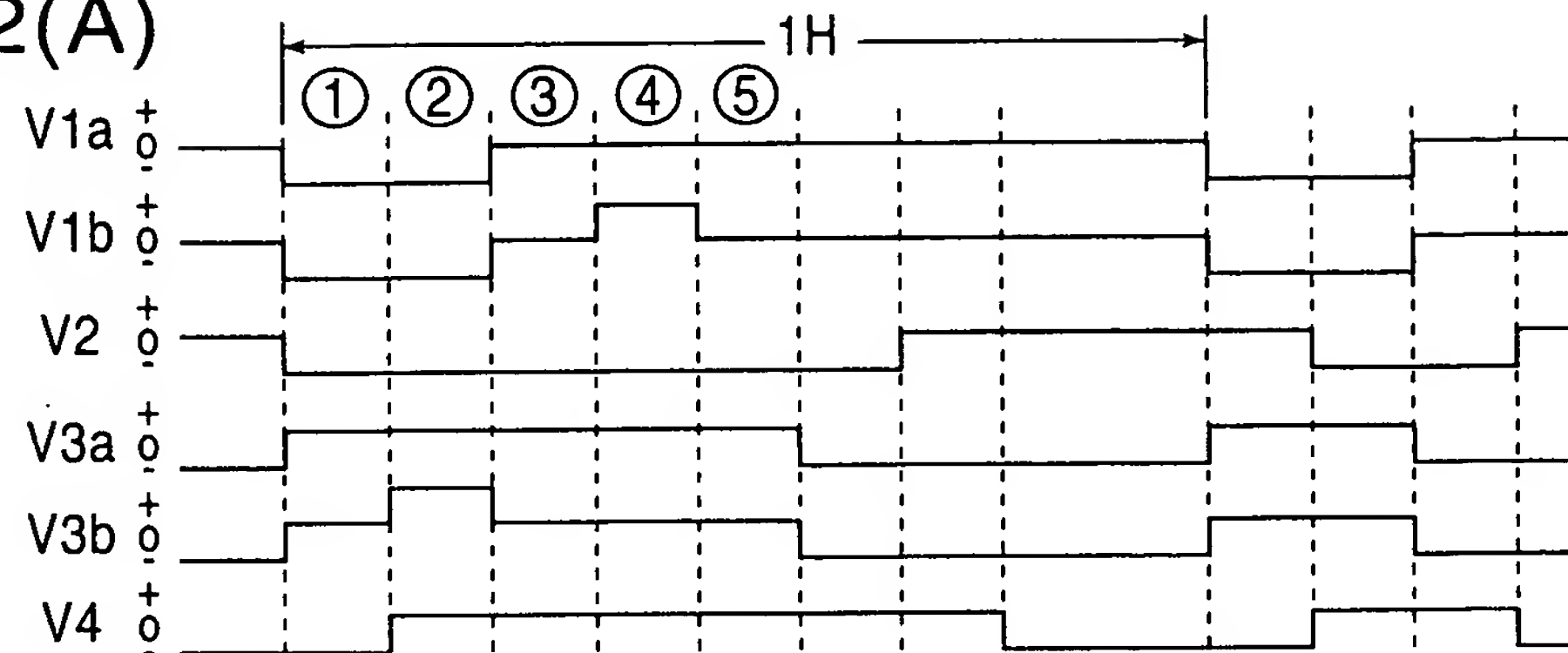
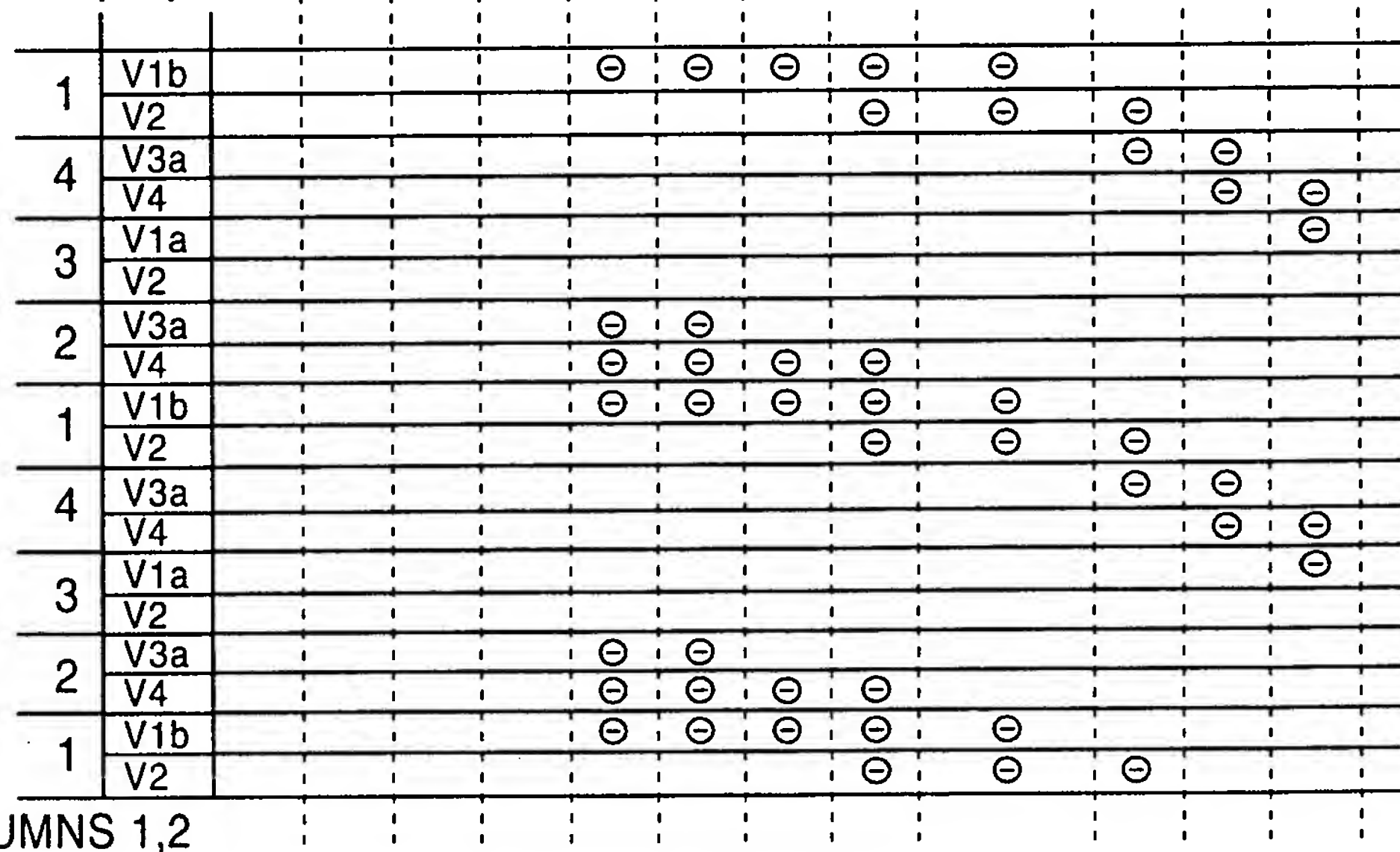
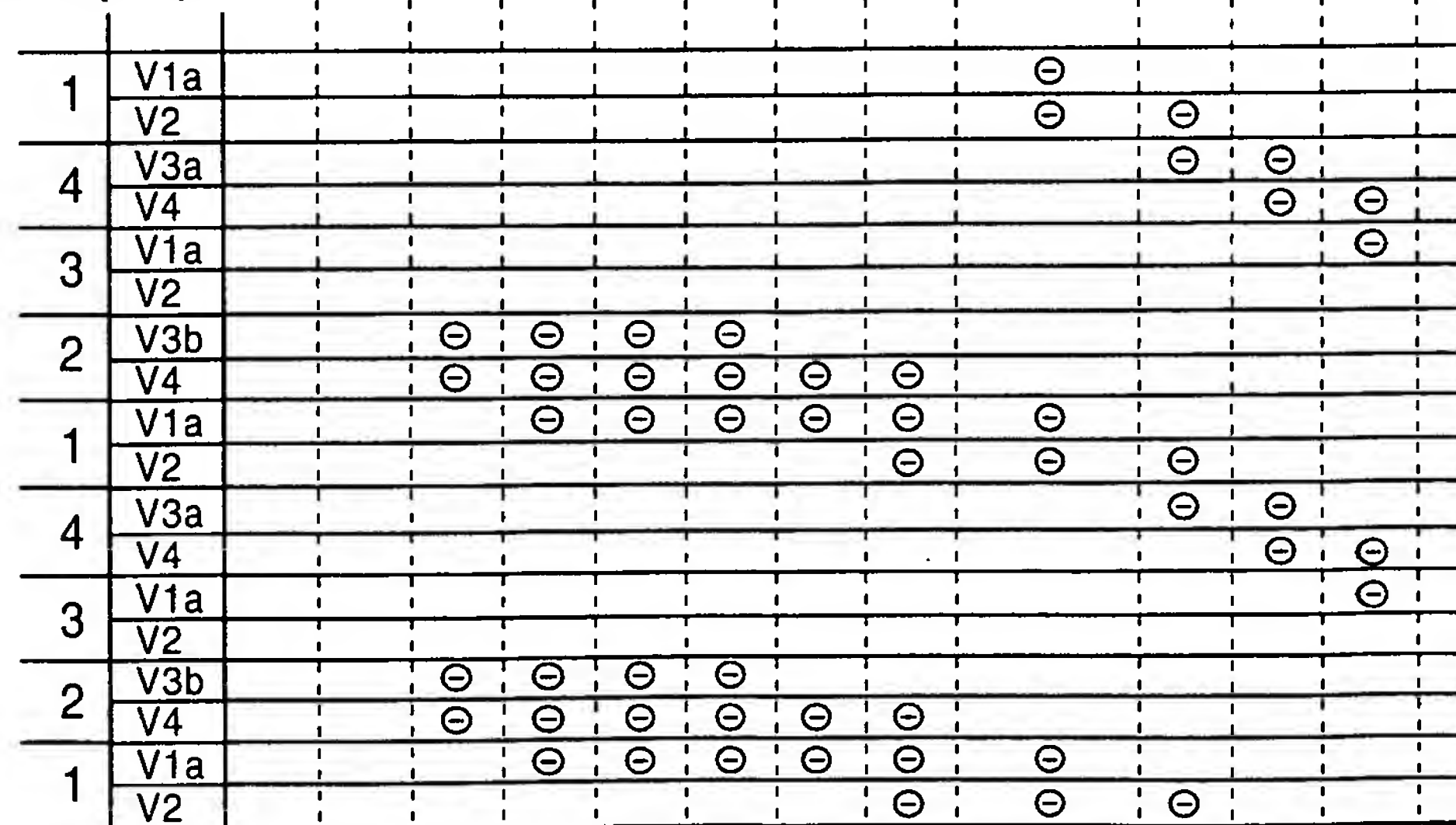


FIG.22(B)



COLUMNS 1,2

FIG.22(C)



COLUMNS 3, 4

FIG. 23

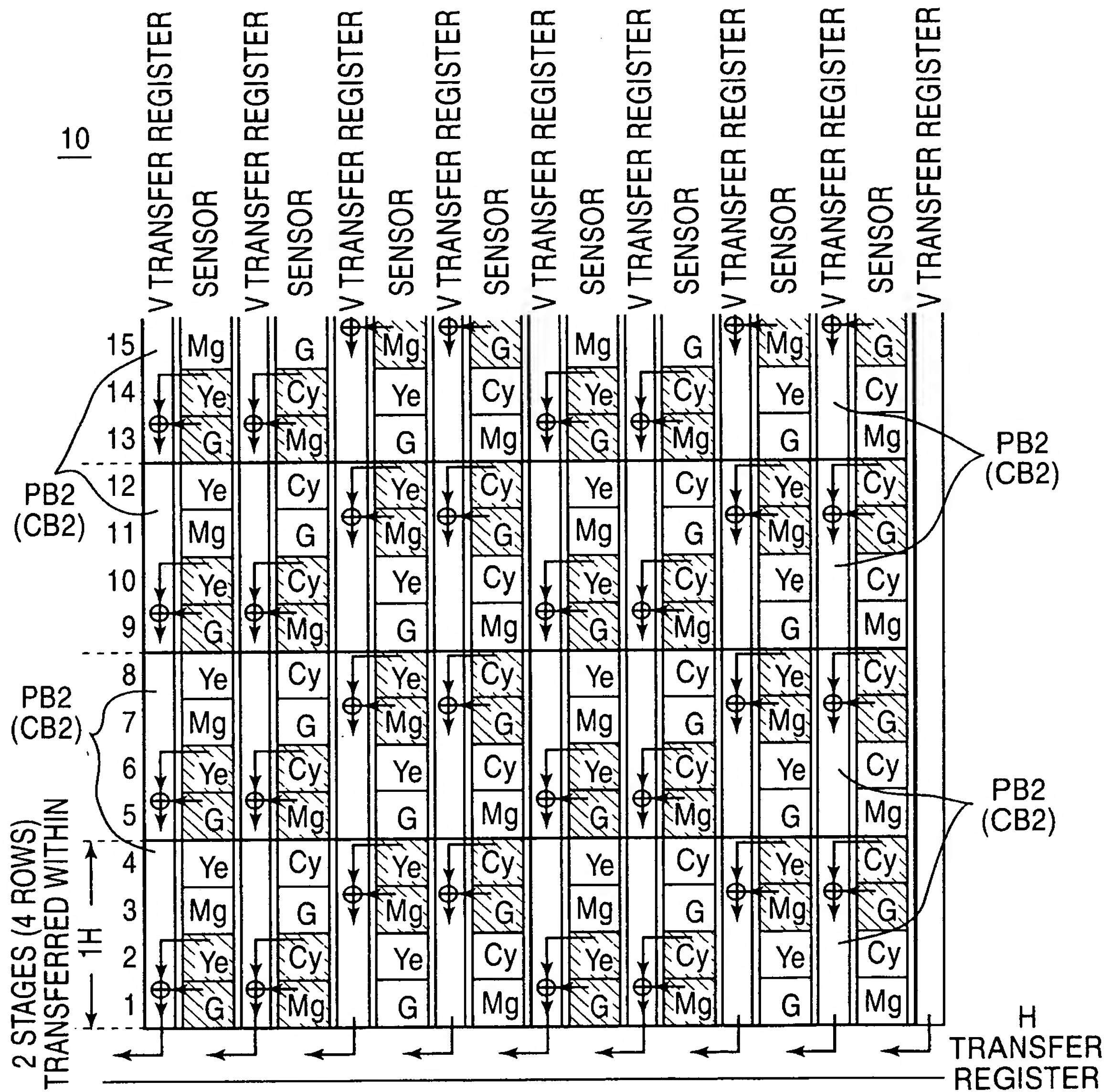




FIG. 24(B)

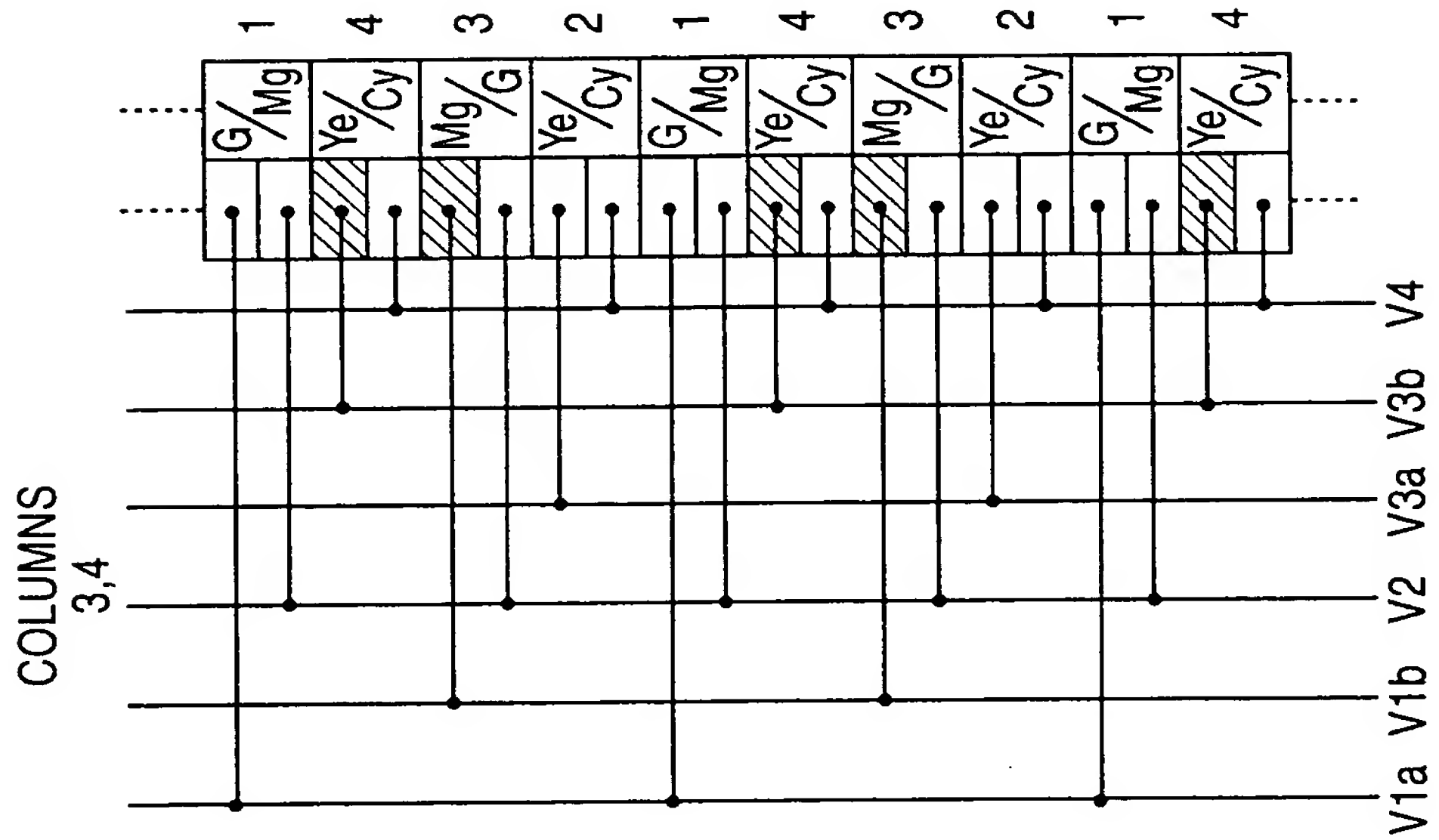


FIG. 24(A)

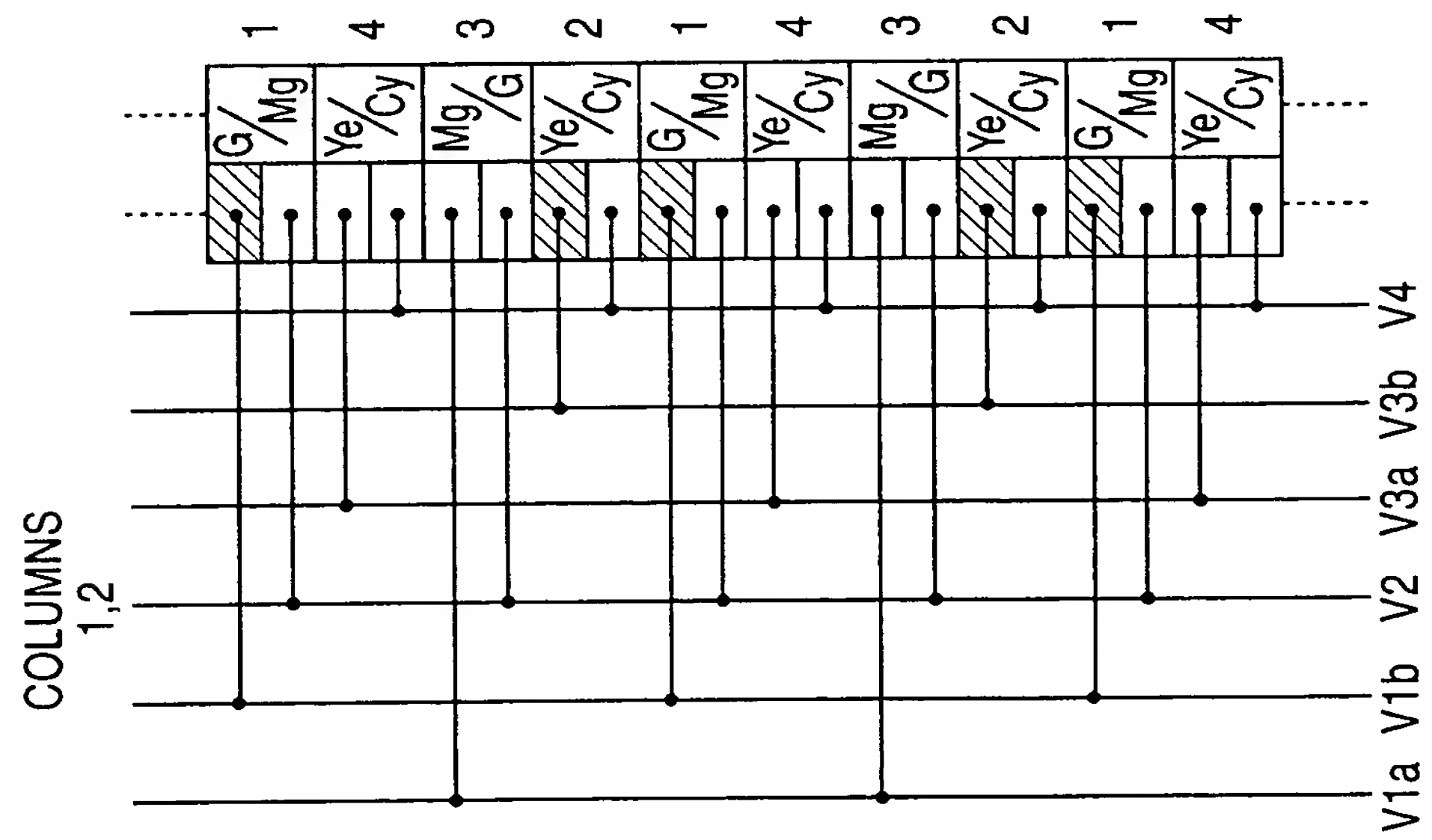




FIG.25(A)

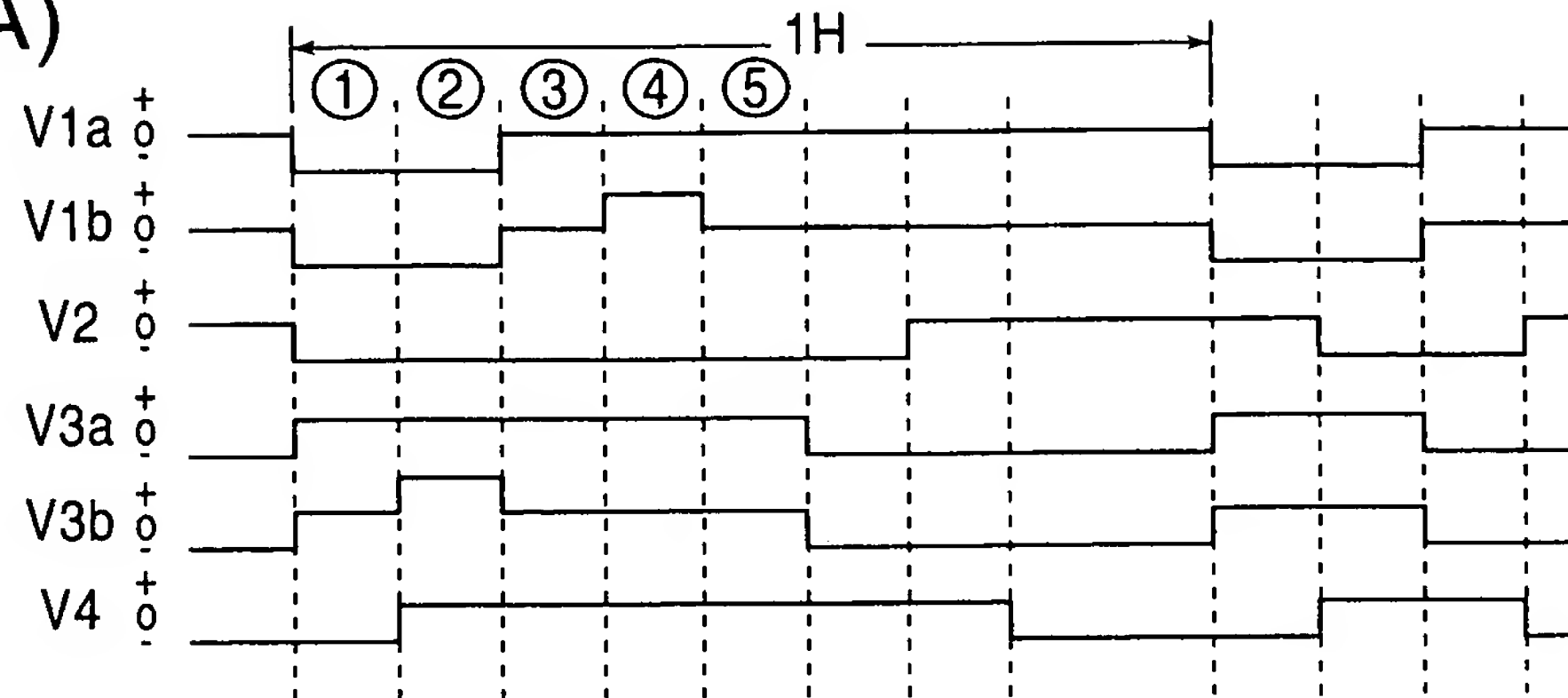
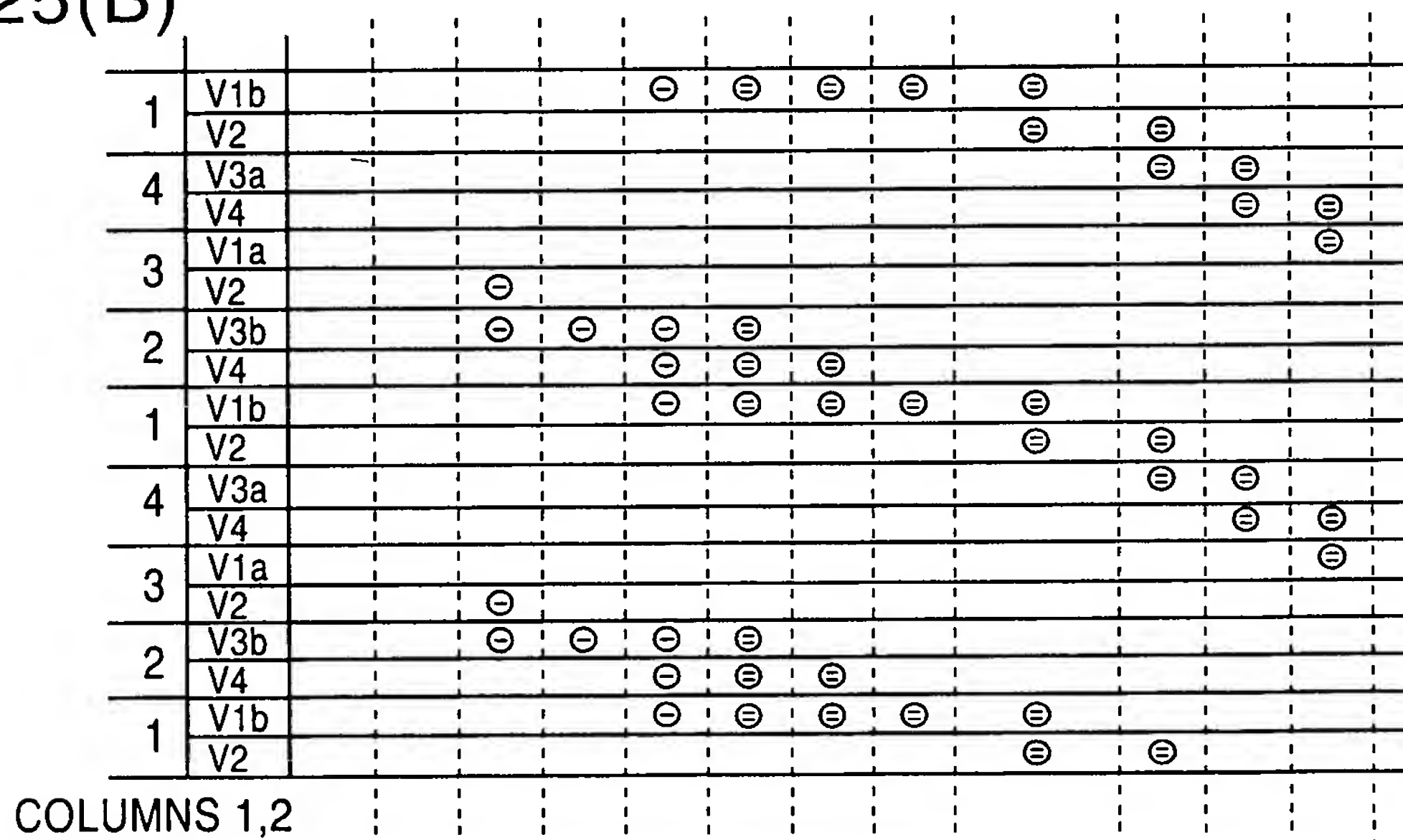
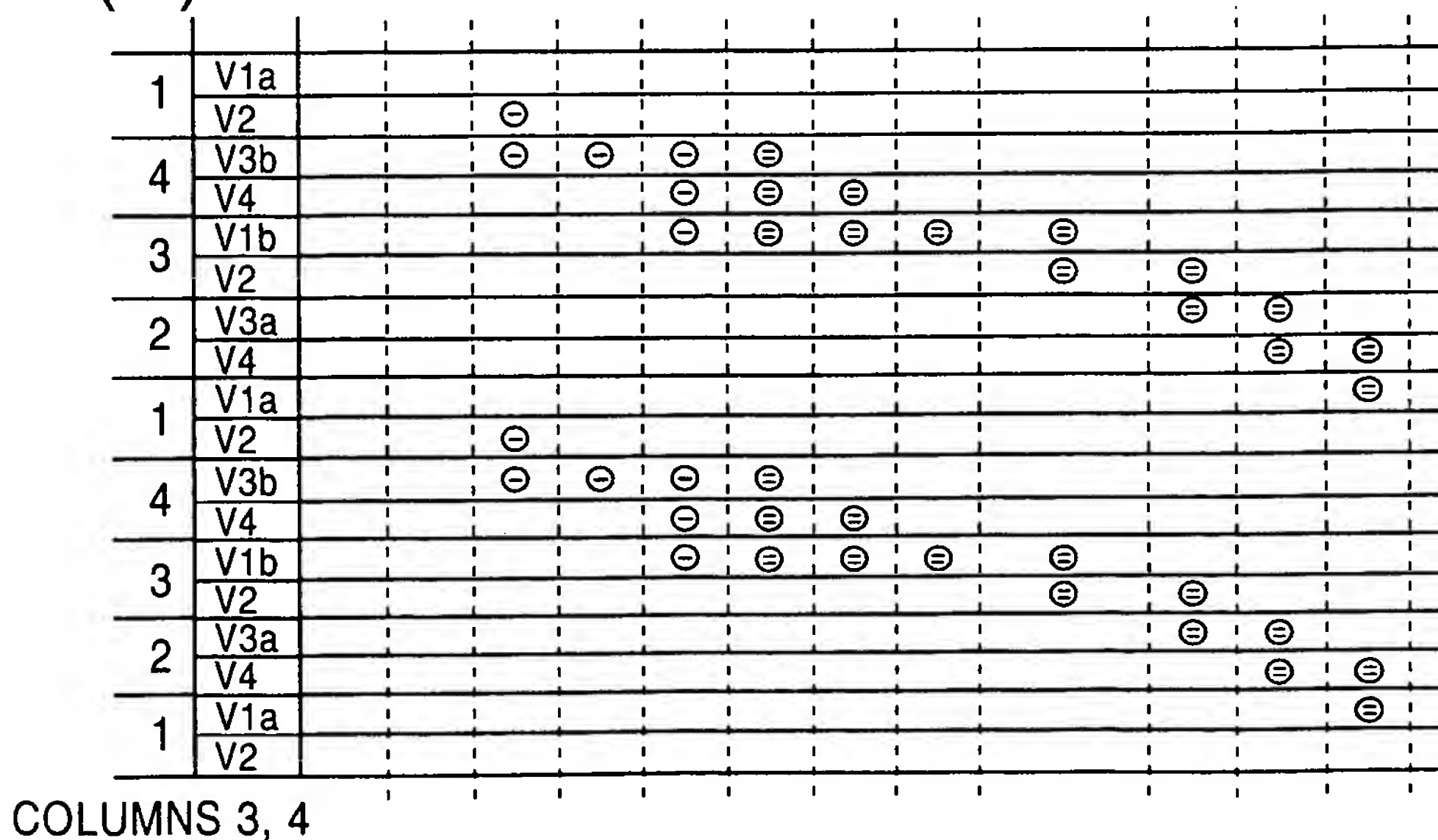


FIG.25(B)



COLUMNS 1,2

FIG.25(C)



COLUMNS 3, 4

Figure 1 is a schematic diagram of a 15-row CCD array. The array is organized into columns labeled "V TRANSFER REGISTER", "SENSOR", and "H TRANSFER REGISTER". Rows are numbered 1 to 15. A vertical dashed line at row 12 is labeled "PB3 (CB3)". A horizontal dashed line at column 1 is labeled "PB3 (CB3)". The diagram shows the sequence of charge transfer and storage in the array.

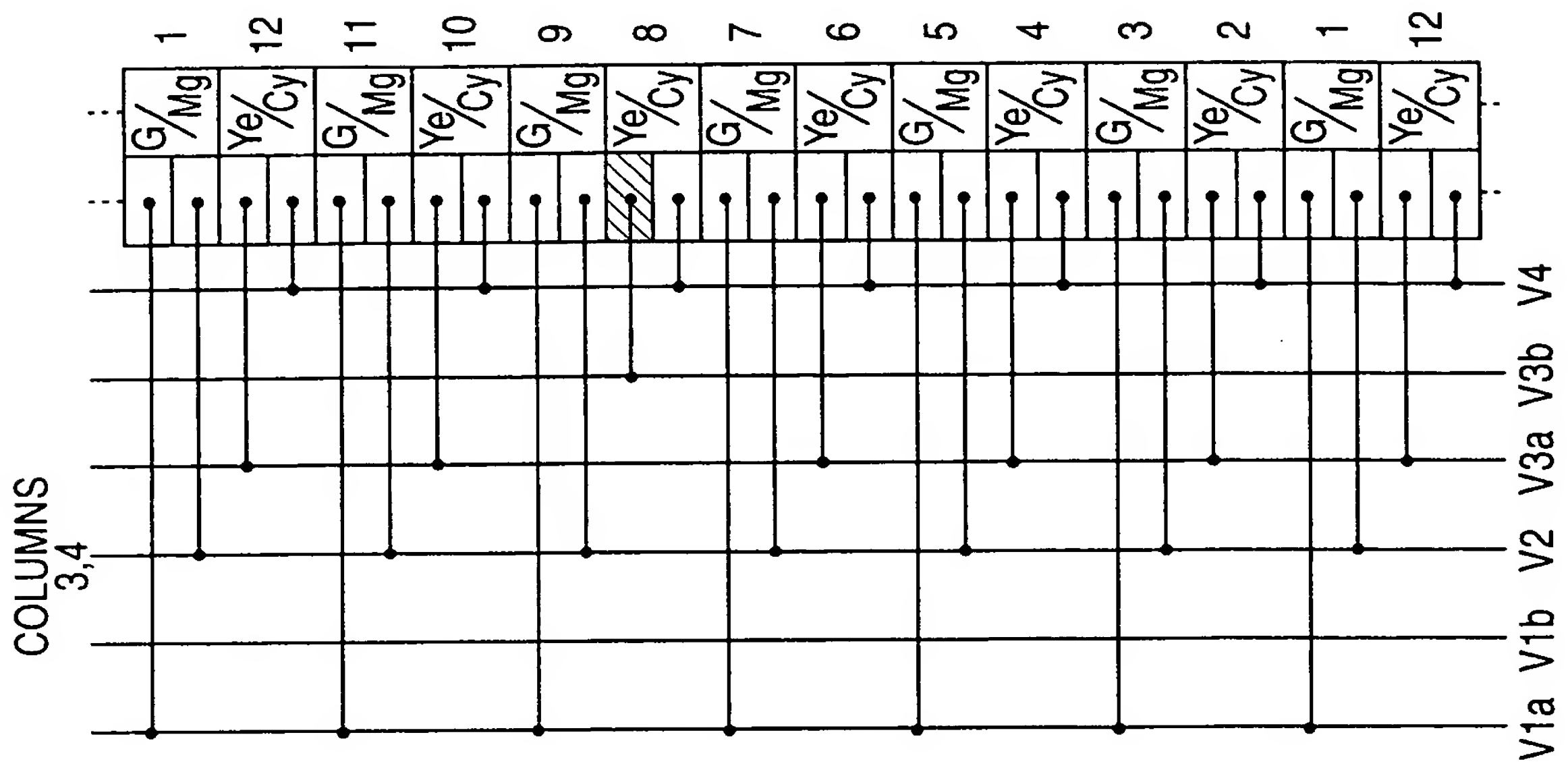


FIG. 27(B)

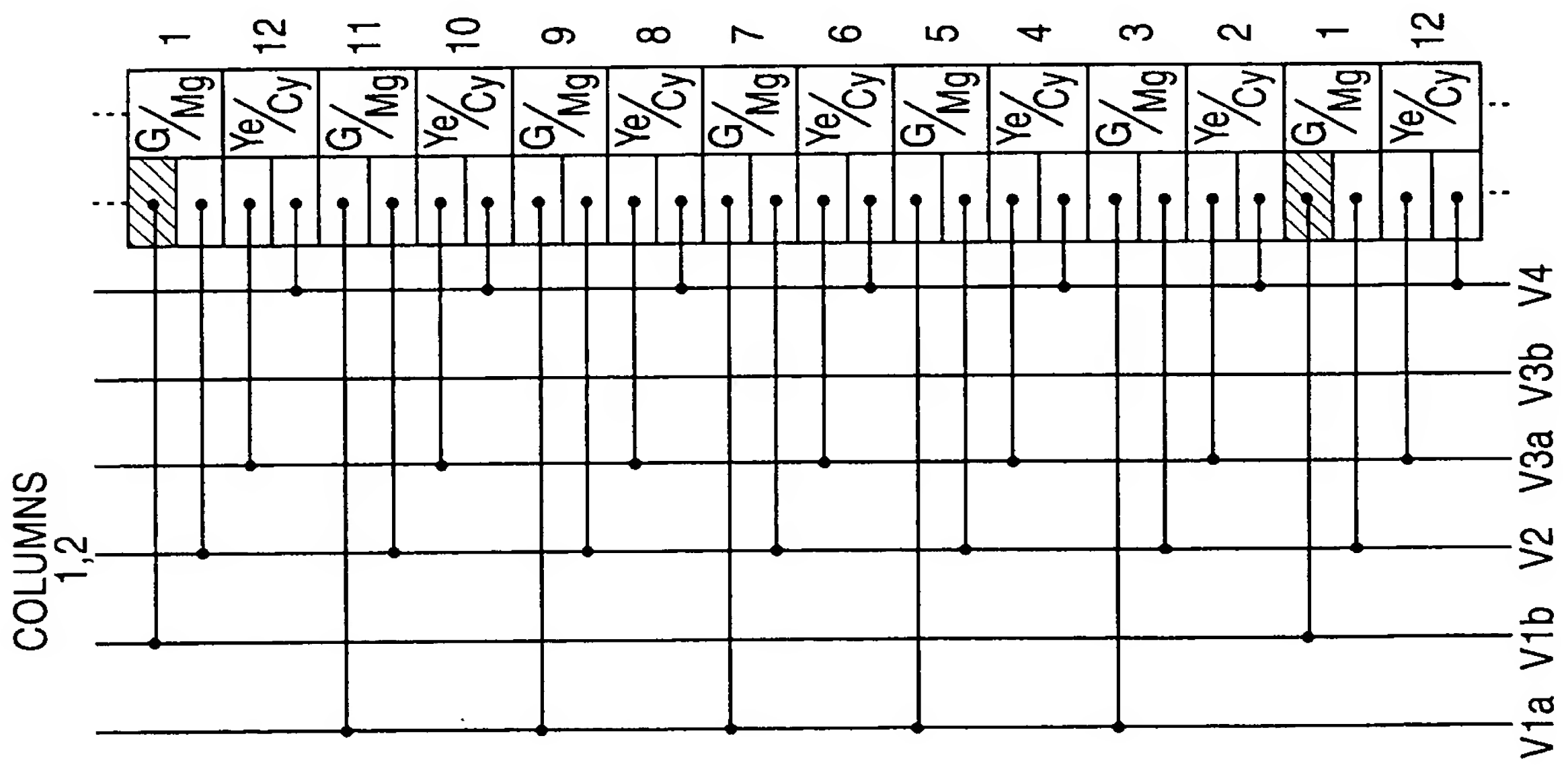


FIG. 27(A)

FIG.28(A)

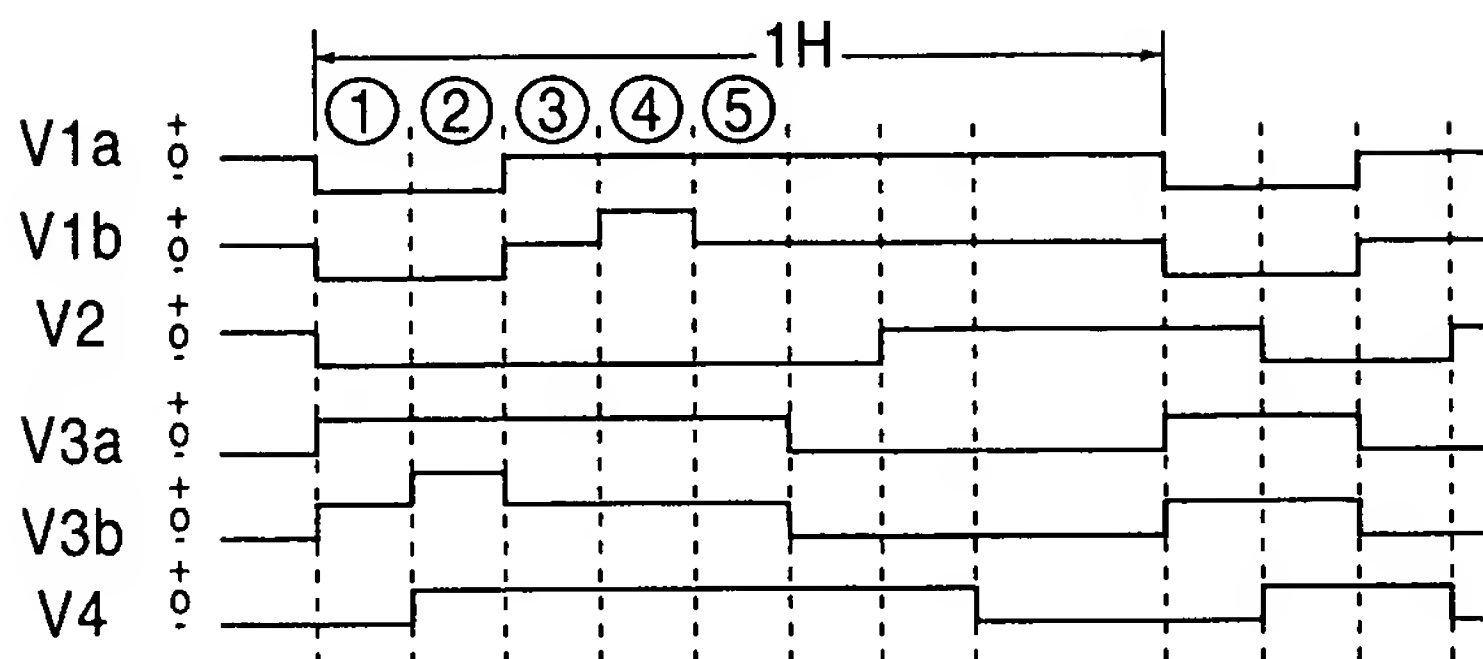


FIG.28(B)

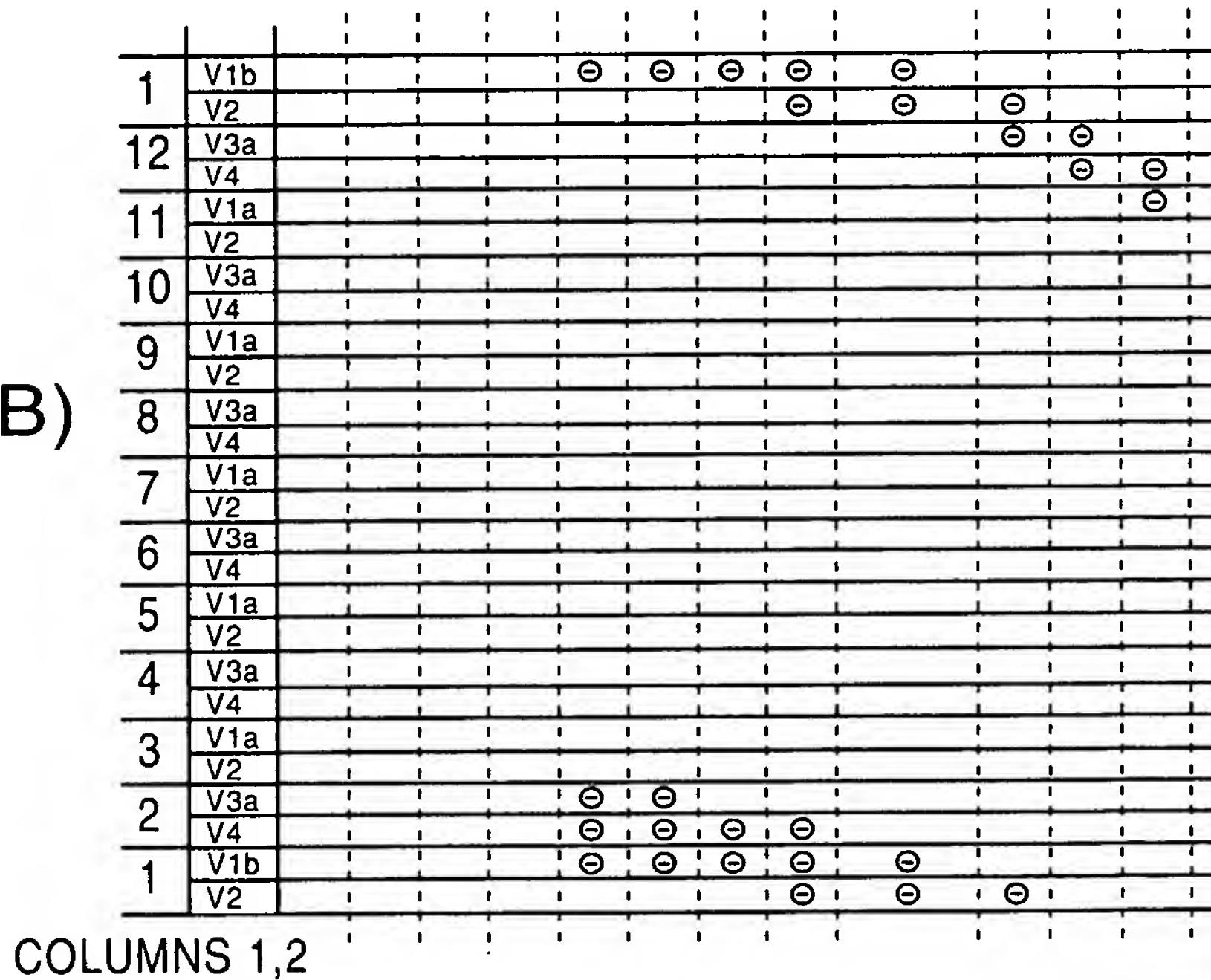


FIG.28(C)

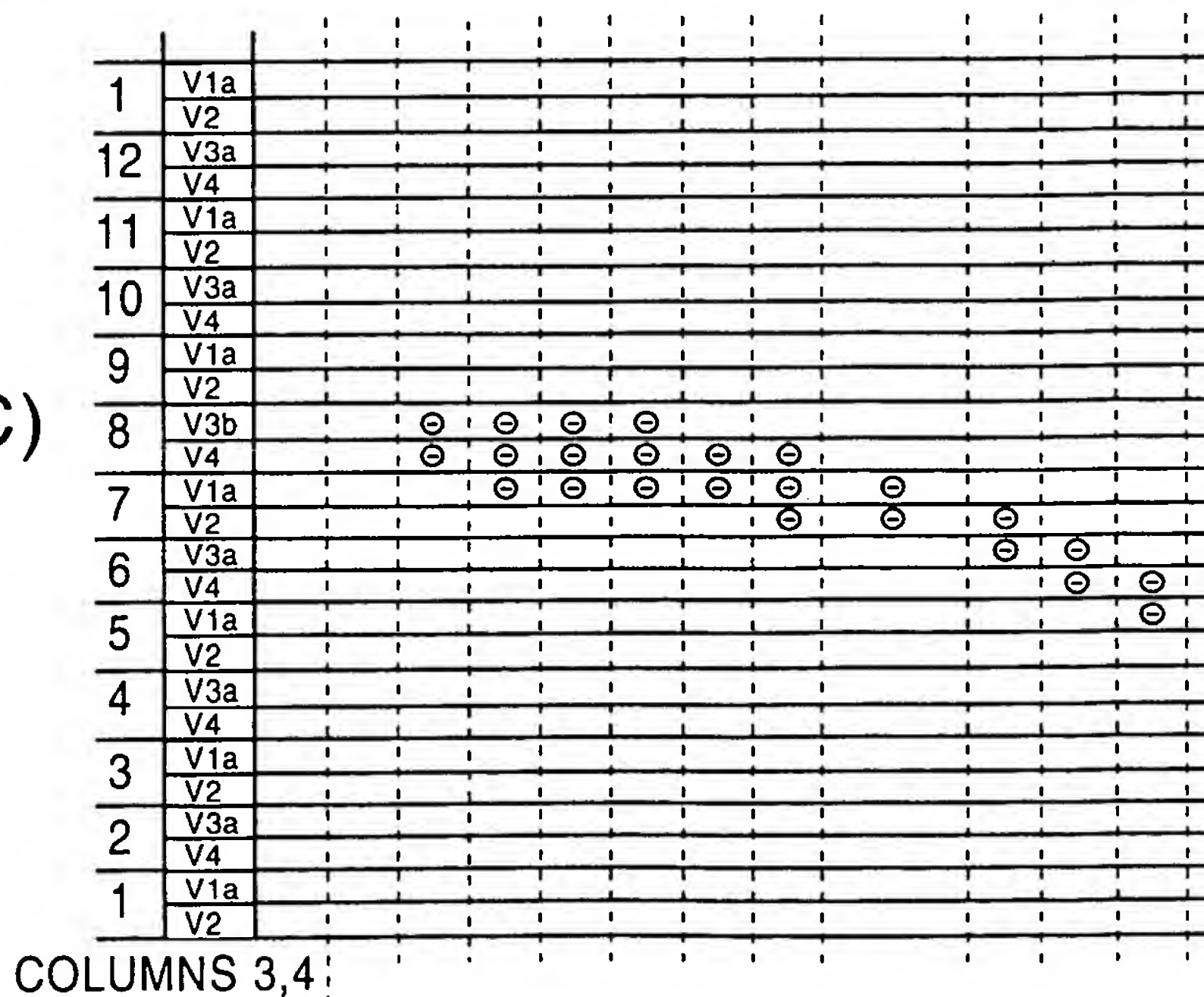


FIG.29

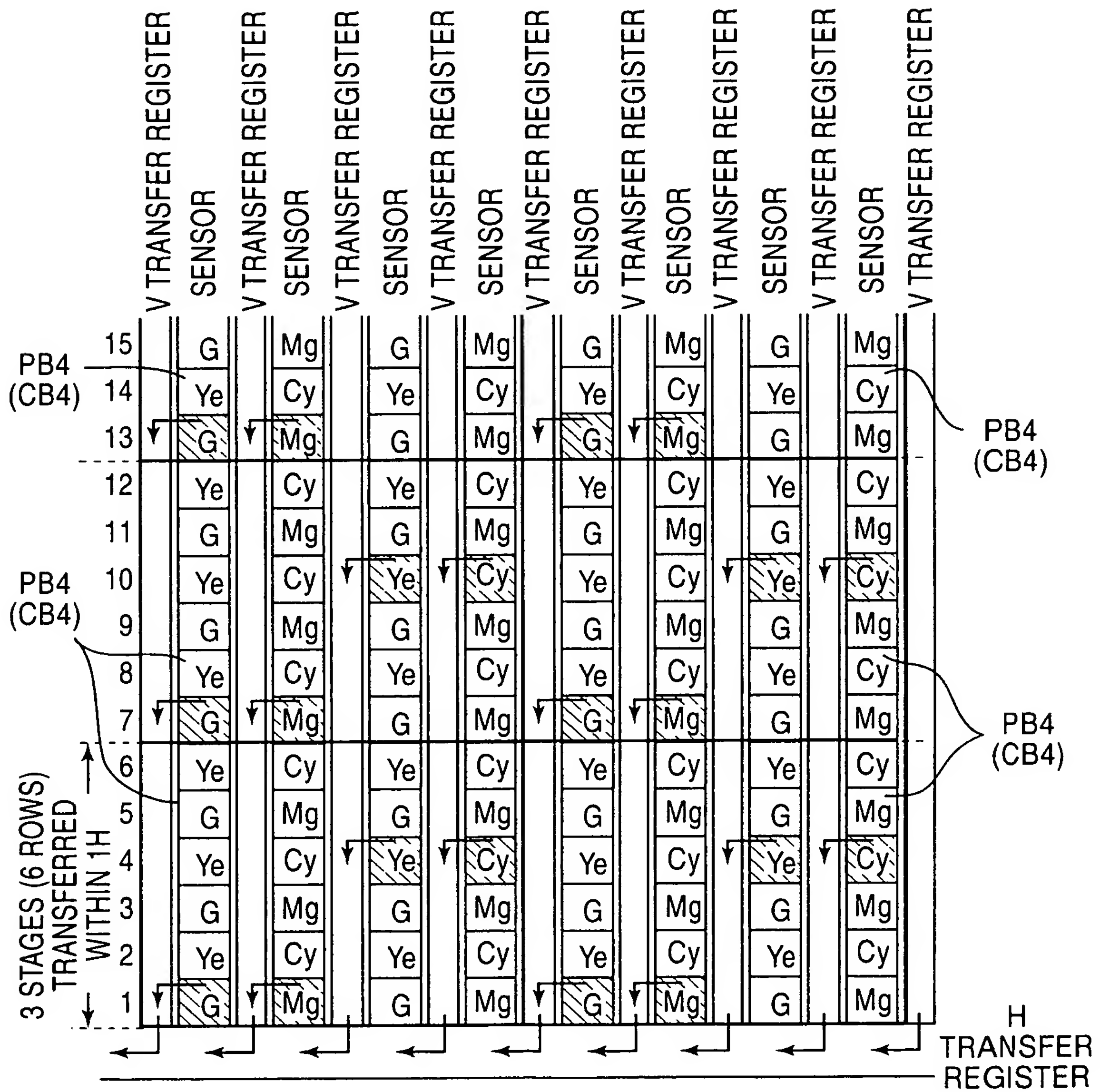


FIG.30(A)

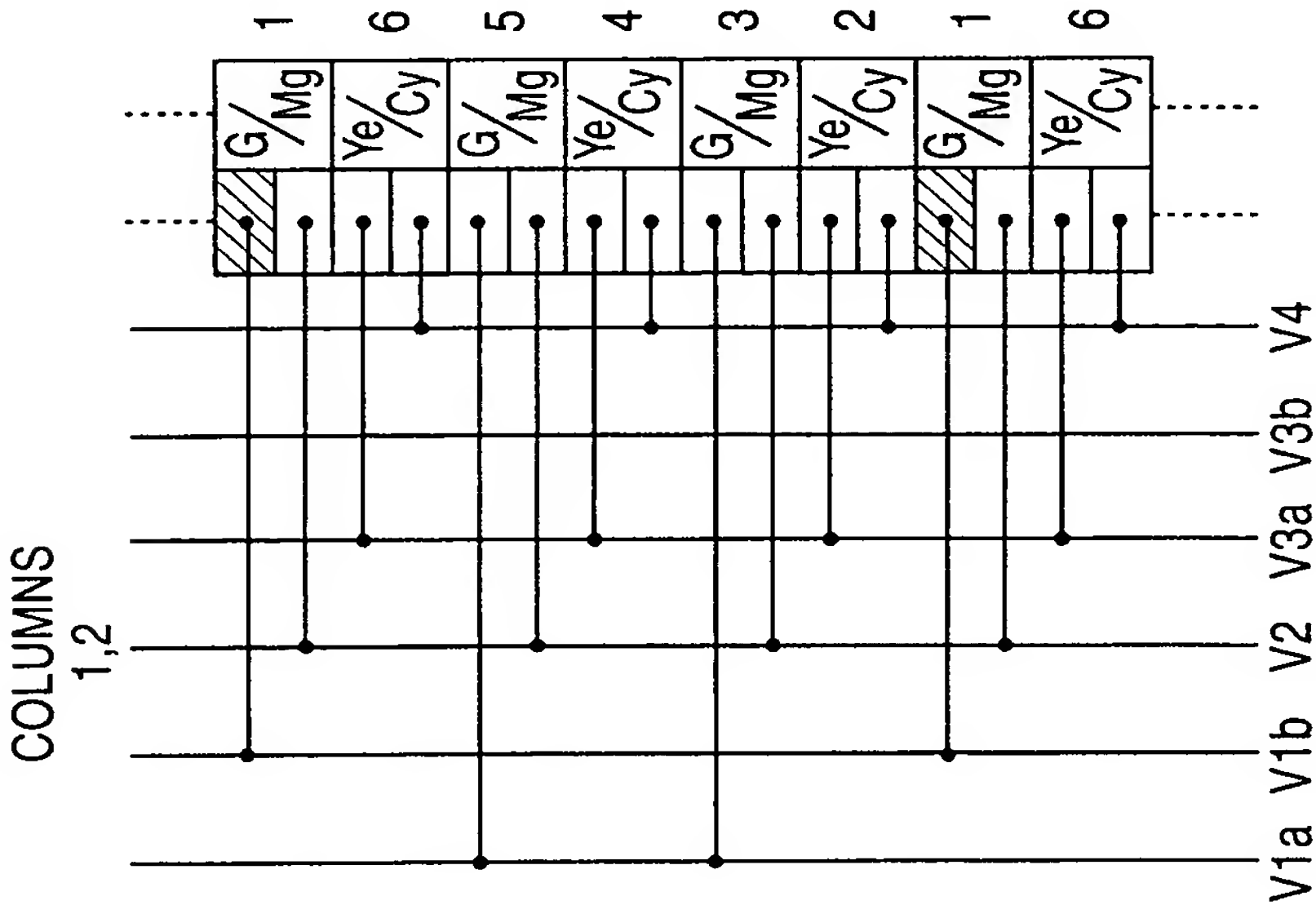


FIG.30(B)

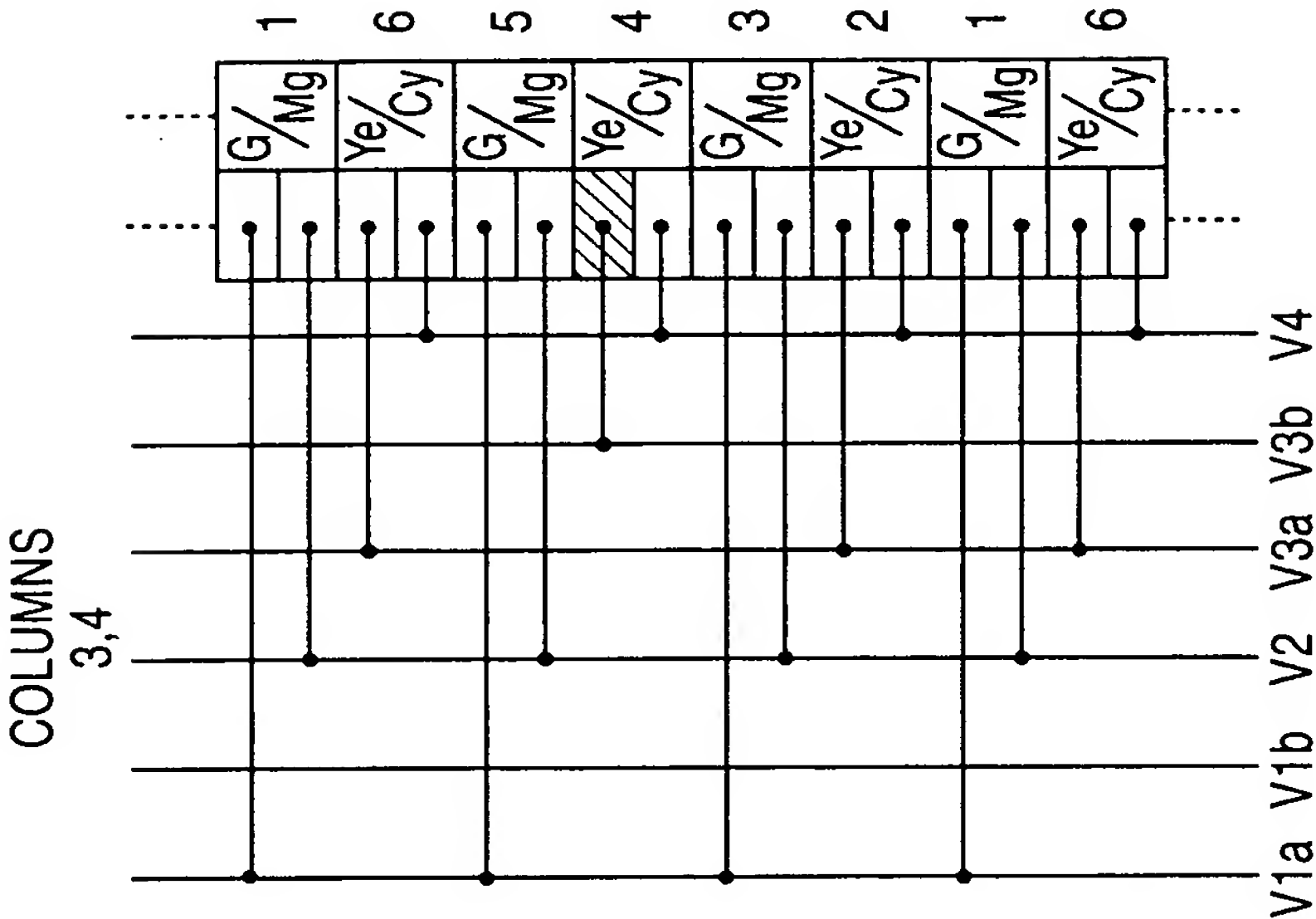




FIG.31(A)

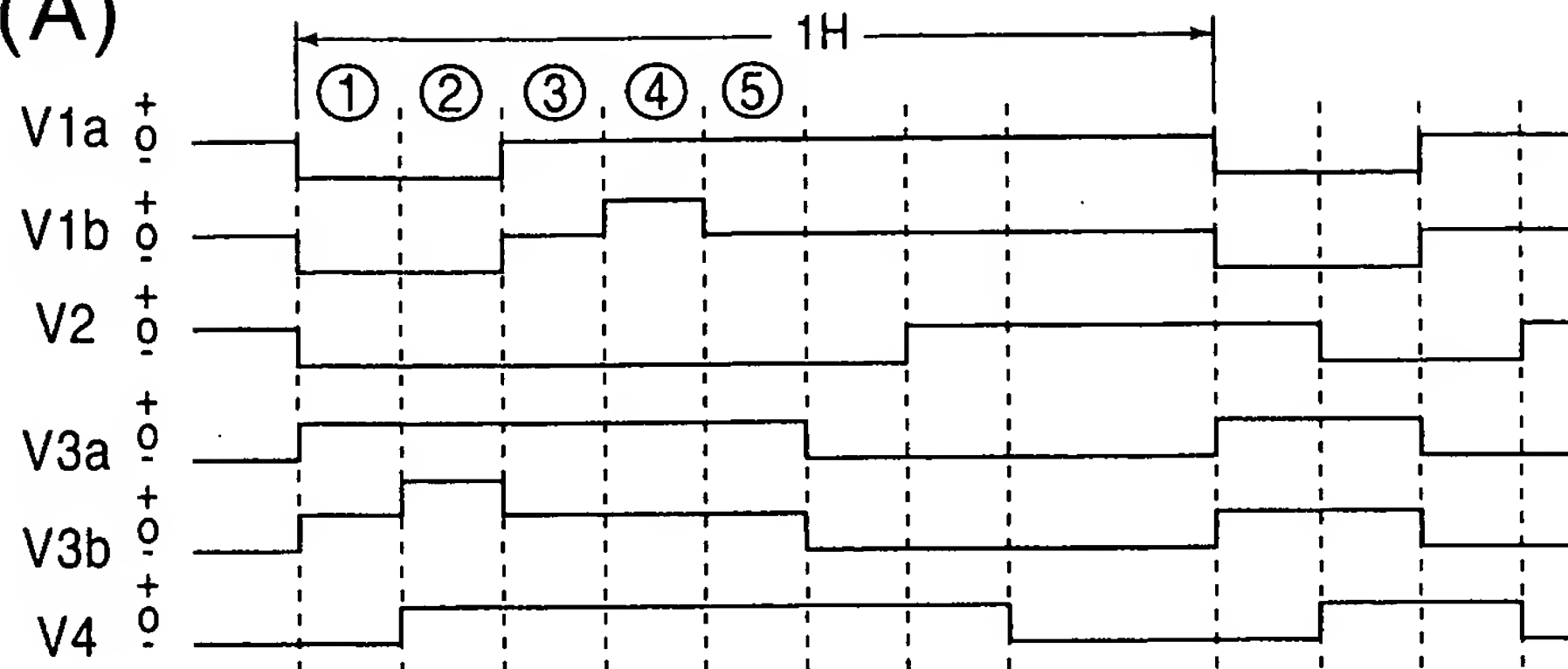


FIG.31(B)

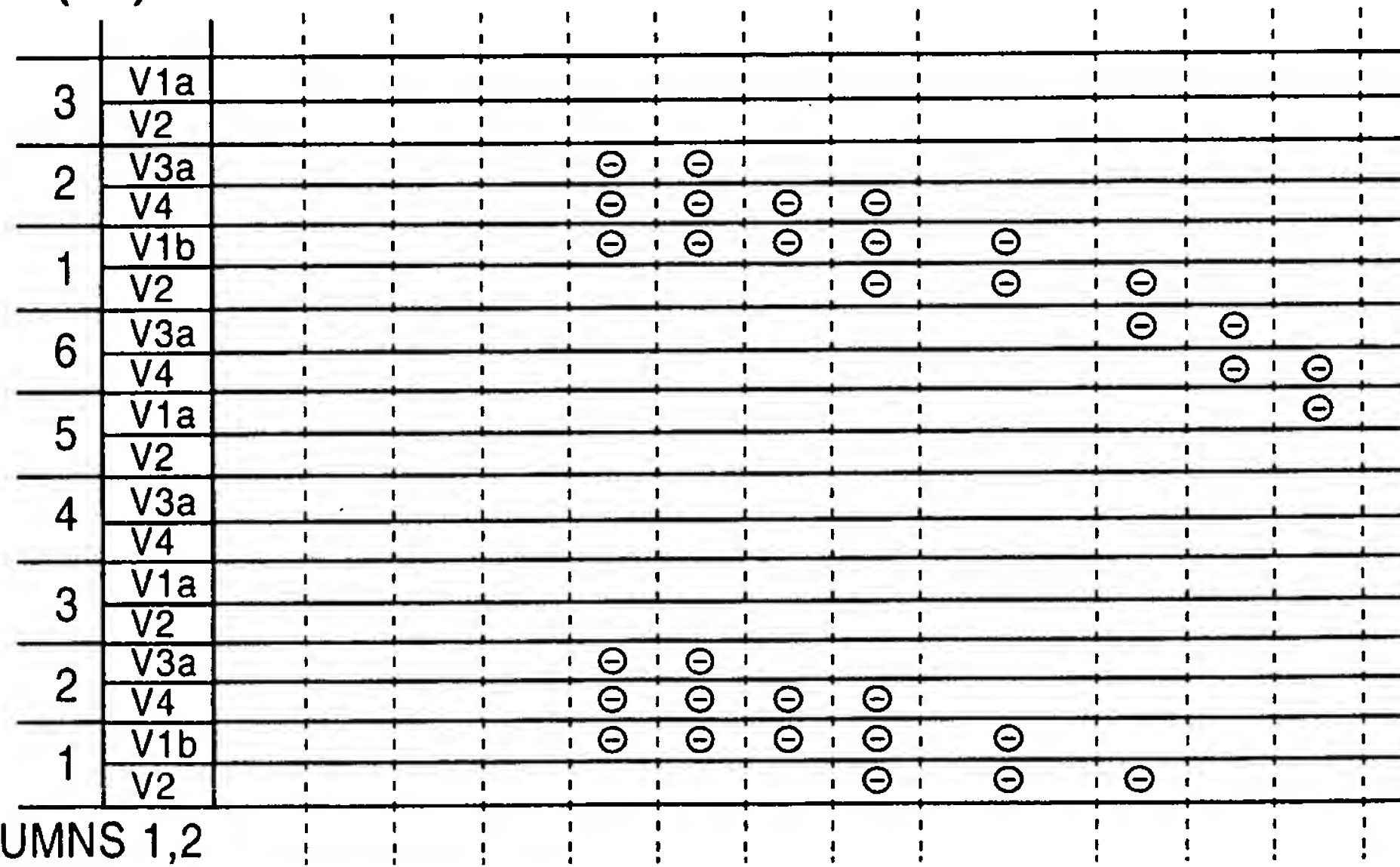


FIG.31(C)

